# CHAPTER-5. POWER ELECTRONICS

**[1]** A 240V, 50Hz supply feeds a highly inductive load of 50 Ohm resistance through a half controlled thyristor bridge. When the firing angle α=45°, the load power is

**A.** 418 W
**B. 512 W**
**C.** 367 W
**D.** 128 W

**Exp:** Vav = (Vm/π) (1 + cosα) = **[**(√2*240)/(π) ) ( 1 + cos45)**]** = 184.4 V
Iav = Vav / R = 184.4/50 =3.69A

$$I_{rms} = I_{av}\sqrt{(\pi - \alpha)/\pi}$$

= 3.69 * √**[**(180 -45)/180**]**
= 3.2A
P = 3.2 * 3.2 *50 = 512 W

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**[**2**]** A **D.C.** to **D.C.** chopper operates from a 48 V battery source into a resistive load of 24Ohm. The frequency of the chopper is set to 250Hz. When chopper on-time is 1 ms the load power is

**A.** 6W
**B.** 12W
**C. 24W**
**D.** 48W

**Exp:** Vavg = V* f * Ton = 48 x 250 x (10 - 3) = 12V
Iav = Vav/R = 12/24 = 0.5A
Vrms= V* Square root (Ton) * f = 48 * Square root (0.25) = 24V
Irms = Vrms/R = 24/24 = 1A
P = Irms * Irms * R = 1 * 24 = 24W

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**[**3**]** A thyristor half wave controlled converter has a supply voltage of 240V at 50Hz and a load resistance of 100 Ohm. when the firing delay angle is 30 the average value of load current is

**A.** 126A
**B.** 2.4A
**C. 126mA**
**D.** 24 A

**Exp:**We know the output wave form of the half wave rectifier For any delay angle alpha, the average load voltage is given by

$$V_{av} = (1/2\pi)\int_{\alpha}^{\pi} E_m \sin\theta\, \delta\theta$$

solving,

$$\boxed{V_{av} = (E_m/2\pi)(1 + \cos\alpha)}$$

substituting the values in the above equation,
Vav = (√2*240) / (2π) * **[** 1 + cos30 **]** = 100.8 V
Iav = Vav/R = 100.8/100 = 126 mA

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**[**4**]** A full-wave fully controlled bridge has a highly inductive load with a resistance of 55 Ohm, and a supply of 110V at 50Hz. The value of load power for a firing angle α=75° is

**A.** 10W
**B.** 11W
**C.** 10.5W

**D. 10.9W**

**Exp:**
Vav = **[**2Vm/(π)**]**cosα**]**
= **[**(2 *√(2*110)/ 3.14 **]** * cos 75
= 99 cos 75
= 25.6V
Iav = Vav / R
= 25.6/55
= 0.446A = Irms

P = Irms * Irms * R
= 0.446 * 0.446 * 55
=10.9W

.....

**[**5**]** A **D.C.** to **D.C.** chopper operates from a 48 V source with a resistive load of 24Ohm. The chopper frequency is 250Hz. When Ton= 3 ms, the rms current is

**A.** 1.5A
**B.** 15mA
**C. 1.73A**
**D.** 173mA

**Exp:** Vav = V *f * Ton = 48 * 250 * 3 *(10 - 3) = 36V
Iav = Vav/R = 36/24 = 1.5 A
Vrms = V* Square root (Ton) * f = 48 * √0.75 = 41.6V
Irms = Vrms/R = 41.6/24 = 1.73A

.....

**[**6**]** A 240V, 50Hz supply feeds a highly inductive load of 50 Ohm resistance through a thyristor full control bridge. when the firing angle α= 45°, load power is

**A.** 456 W
**B. 466 W**
**C.** 732 W
**D.** 120 W

**Exp:** Vav = (2Vm/π) * cosα = **[**(2 * 339)/3.14**]** cos 45 = 152.6V
Iav = Vav/R = 152.6 / 50 = 3.05A = Irms
P = Square of Irms * R = 3.04 * 3.04 * 50 = 466W

.....

[7] Thermal runaway is not possible in FET because as the temperature of FET increases

**A. The mobility decreases**
B. The transconductance increases
C. The drain current increases
D. None of the above

[8] The ripple frequency from a full wave rectifier is

A. twice that from a half wave circuit
B. the same as that from a half wave circuit
C. half that from a half wave circuit
D. 1/4 that from a half wave circuit

[9] In a full-wave rectifier using two ideal diodes,Vdc & Vm are the dc & peak values of the voltage respectively across a resistive loaD. If PIV is the peak inverse voltage of the diode,then the appropriate relationships for the rectifier is

A. $V_{dc}$=Vm/π,PIV=2Vm
**B. $V_{dc}$=2Vm/π,PIV=2Vm**
C. $V_{dc}$=2Vm/π,PIV=Vm
D. $V_{dc}$=Vm/π,PIV=Vm

**[**10**]** The output of a rectifier circuit without filter is

**A.** 50 Hz AC
**B.** smooth DC
**C. pulsating DC**
**D.** 60 hz AC

**[**11**]** An advantage of full wave bridge rectification is
**A. it uses the whole transformer secondary for the entire ac input cycle**
**B.** it costs less than other rectifier types
**C.** it cuts off half of the ac wave cycle
**D.** it never needs a filter

**[**12**]** The best rectifier circuit for the power supply designed to provide high power at low voltage is
**A.** half wave arrangement
**B. full wave, center tap arrangement**
**C.** quarter wave arrangement
**D.** voltage doubler arrangement

**[**13**]** If a half wave rectifier is used with 165Vpk AC input, the effective dc output voltage is
**A. considerably less than 165V**
**B.** slightly less than 165V
**C.** exactly 165V
**D.** slightly more than 165V

**[**14**]** If a full wave bridge circuit is used with a transformer whose secondary provides 50Vrms, the peak voltage that occurs across the diodes in the reverse direction is approximately
**A.** 50 Vpk
**B. 70 Vpk**
**C.** 100 Vpk
**D.** 140 Vpk

**[**15**]** The main disadvantage of voltage doubler power supply circuit is
**A.** Excessive current
**B.** Excessive voltage
**C.** Insufficient rectification
**D. Poor regulation under heavy loads**

**[**16**]** A source follower using an FET usually has a voltage gain which is
**A. Greater than +100**
**B.** Slightly less than unity but positive
**C.** Exactly unity but negative
**D.** About -10

**[**17**]** The average output voltage(Vdc) of the full wave diode bridge rectifier is
**A.** Vm/2
**B. 2Vm/pi**
**C.** 3Vm/pi
**D.** 4Vm/pi

**[**18**]** The typical ratio of latching current to holding current in a 20A thyristor is **[GATE -2011]**
**A.** 5.0
**B. 2.0**
**C.** 1.0
**D.** 0.5

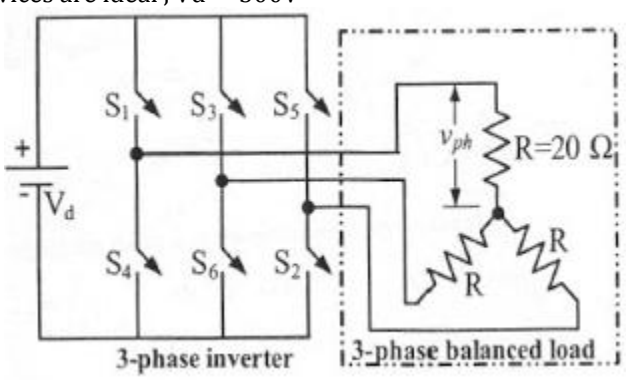
**[**19**]** A half controlled single phase bridge rectifier is supplying an R-L loa**D.** It is operated at a firing angle (alpha) and load current is continuous. The fraction of cycle that the freewheeling diode conducts is **[GATE -2011]**

(A) $\frac{1}{2}$ (B) $\left(1-\frac{\alpha}{\pi}\right)$ (C) $\frac{\alpha}{2\pi}$ (D) $\frac{\alpha}{\pi}$

**Ans: D**

**Common Data for Questions [20] & [21]**

In the 3 phase inverter circuit shown, the load is balanced and the gating scheme is 180 degree conduction mode. All the switching devices are ideal , Vd = 300V




**[20]** The rms value of load phase voltage is **[GATE -2011]**

**A.** 106.1V
**B. 141.4 V**
**C.** 212.2 V
**D.** 282.8V

**HINT:-** VL = Square root(2/3) * Vs

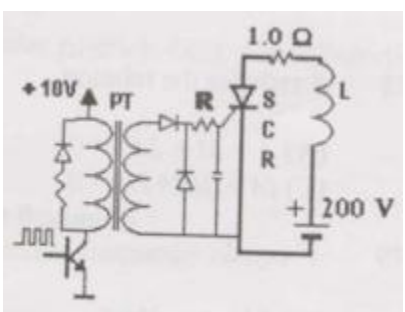
**[21]** If the dc bus voltage Vd = 300v, the power consumed by 3 phase load is **[GATE -2011]**

**A.** 1.5kW
**B.** 2.0 kW
**C.** 2.5 kW
**D. 3.0 kW**

**HINT:-** P = 3 * **[**(Vph * Vph)/Rph**]**

**Common Data for Question 22 & 23:**

1 Pulse Transformer (PT) is used to trigger the SCR in the adjacent figure. The SCR is rated at 1.5KV, 250A with IL=250mA, IH=150mA, and IGmax= 150mA, IGmin=100m**A.** The SCR is connected to an inductive load, where L=150mH in series with a small resistance and the supply voltage is 200V d**C.** The forward drops of all transistors/ diodes and gate- cathode junction during ON state are 1.0V.




**[22]** The resistance R should be

(a) 4.7K Ohm
(b) 470 Ohm
**(c) 47 Ohm**
(d) 4.7 Ohm

**[23]** The minimum approximate volt-second rating of the pulse transformer suitable for triggering the SCR should be: ( volt-second rating is the maximum of product of the voltage and the width of the pulse that may be applied

**(a) 2000 uV-s**
(b) 200 uV-s

(c) 20 uV-s
(d) 2.0 uV-s

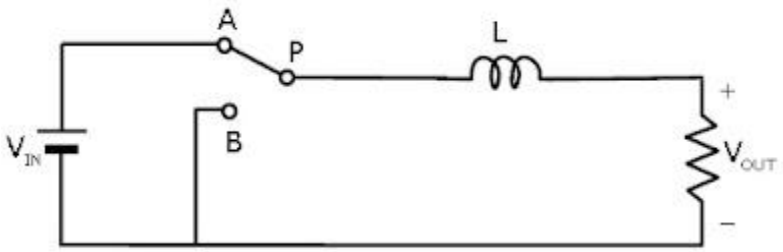
**[**24**]** " Six MOSFETs connected in a bridge configuration (having no other power device) MUST be operated as a Voltage Source Inverter (VSI) ". This statement is **[GATE-2007]**

**A.** True, because being majority carrier devices, MOSFETs are voltage driven
**B.** True, because MOSFETs have inherently anti parallel diodes
**C.** False, because it can be operated both as current source Inverter (CSI) or a VSI
**D. False, because MOSFETs can be operated as excellent constant current sources in the saturation region**

**[**25**]** A single phase full - wave half controlled bridge converter feeds an inductive loa**D.** The two SCRs in the converter are connected to a common DC bus. The converter has to have a free wheeling diode **[GATE-2007]**

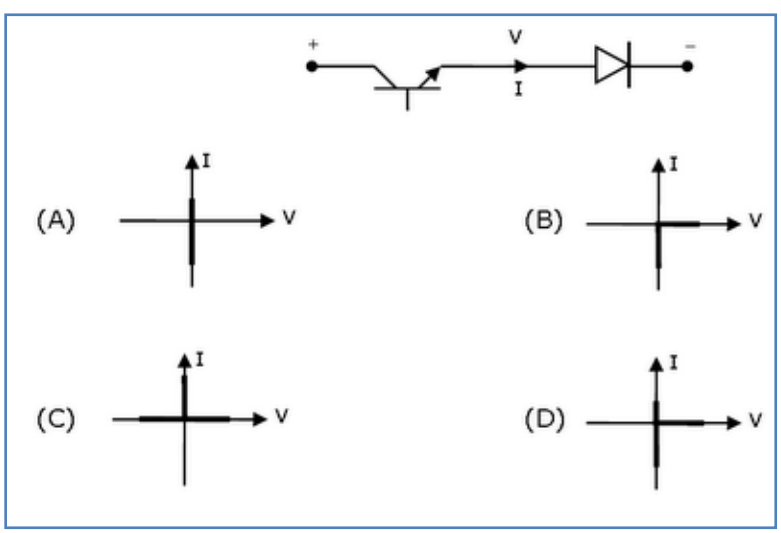
**A.** because the converter inherently does not provide for free wheeling
**B. Because the converter does not provide for freewheeling for high values of triggering angles**
**C.** Or else the freewheeling action of the converter will cause shorting of the AC supply
**D.** Or else if a gate pulse to one of the SCRs is missed, it will subsequently cause a high load current in the other SCR

**[**26**]** The power electronic converter shown in the figure has a single pole double throw switch. the pole P of the switch is connected alternately to throws A and **B.** The converter shown is a **[GATE-2010]**



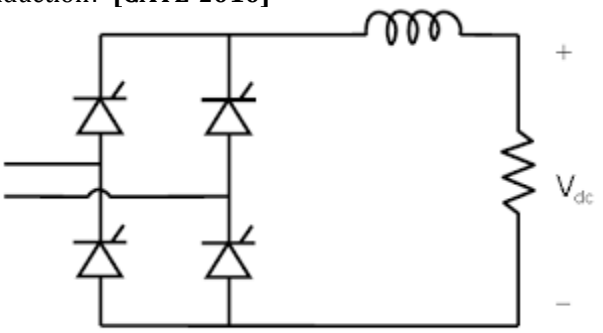

**A. Step down chopper( buck converter)**
**B.** Half- wave rectifier
**C.** Step Up chopper ( boost converter)
**D.** full wave converter

**[**27**]** Figure shows a composite switch consisting of a power transistor (BJT) in series with a diode. Assuming that the transistor switch and the diode are ideal, the I-V characteristic of the composite switch is **[GATE-2010]**




**Ans: C**

**[**28**]** The fully controlled thyristor converter in the figure is fed from a single-phase source. When the firing angle is 0°, the dc output voltage of the converter is 300 V. What will be the output voltage for a firing angle of 60°, assuming continuous conduction? **[GATE-2010]**




**(A) 150V**
(B) 210V
(C) 300V
(D) 100.(pi).V

**[**29**]** The manufacturer of a selected diode gives the rate of fall of the diode current di/dt = 20 A/ms, and a reverse recovery time of trr =5 ms. What is value of peak reverse current?

**Ans: 44.72A**

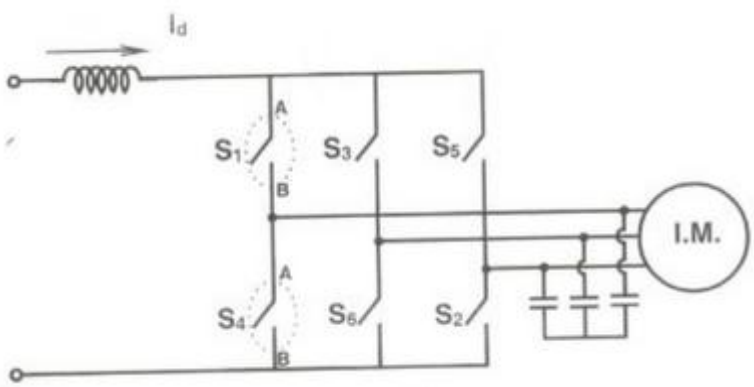
**HINT:-**The peak reverse current is given as:

$$I_{rr} = \sqrt{\frac{di}{dt} 2Q_{RR}}$$

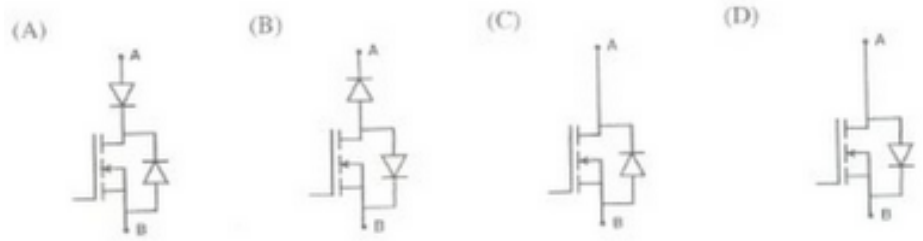
The storage charge QRR is calculated as Qrr = (1/2)*(di/dt)* SQU.(trr)
= 1/2 X 20A/uS X 5u X 5u = 50u**C.**
substitute the Qrr value in Irr equation.

$$I_{rr} = \sqrt{20\frac{a}{\mu s} \times 2 \times 50\ \mu C} = 44.72\ A$$

**[**30**]** A three phase current source inverter used for the speed control of an induction motor is to be realized using MOSFET switches as shown below. Switches S1 to S6 are identical switches **[GATE2011]**



The proper configuration for realizing switches S1 to S6 is




**Ans: C**

**[**31**]** Circuit turn-off time of an SCR is defined as the time **[GATE2011]**

**A.** taken by the SCR to turn off
**B.**required for SCR current to become zero
**C. for which the SCR is reverse biased by the commutation circuit**
**D.** for which the SCR is reverse biased to reduce its current below the holding current

**[**32**]** A single phase fully controlled thyristor bridge ac-dc converter is operating at a firing angle of 25 degree, and an overlap angle 10 degree with constant dc output current of 20**A.** The fundamental power factor ( displacement factor) at input ac mains is **[GATE2007]**

**A. 0.78**
**B.** 0.827
**C.** 0.866
**D.** 0.9

**[**33**]** A three phase fully controlled thyristor bridge converter is used as line commutated inverter to feed 50 KW power at 420 V DC to a three phase 415V(line), 50Hz as mains. Consider Dc link current to be constant. The rms current of the thyristor is **[GATE2007]**

**A.** 119.05A
**B.** 79.37A
**C.** 68.73A
**D. 39.68A**

**[**34**]**which of the following statements are true about VI characteristic of SCR?

**A.** Holding current is more than Latching current
**B.** SCR will trigger if the applied voltage exceeds forward break over voltage
**C.** SCR can be triggered without gate current
**D.** When the SCR is in reverse biased, small leakage current will flow

**Options:**

**A.** A, B and C
**B.** All are true
**C. B, C, D**
**D.** C, D

**[**35**]** which of the following statements are true about BJT?

(i) It has more power handling capability than MOSFET
(ii) Has higher switching speed than IGBT and MOSFET
(iii) Has low on state conduction resistance
(iv) Has second breakdown voltage problem

**Options:**

**A.** All are true
**B.** (i), (ii), (iii) and (iv)
**C. (i), (iii) and (iv)**
**D.** (ii), (iii) and (iv)

**[**36**]** For a JFET, when VDS is increased beyond the pinch off voltage, the drain current

**A.** Increases
**B.** Decreases

**C. Remains constant**

**D.** First decreases and then increases

**[**37**]** n-channel FETs are superior to P-channel FETs, because

**A.** They have higher input impedance

**B.** They have high switching time

**C.** They consume less power

**D. Mobility of electrons is greater than that of holes**

**[**38**]** Which of the following is true about the diodes

**A.** During forward biased small amount of voltage drop will appear across anode and cathode

**B.** If the reverse voltage exceed $V_{RRM}$ the diode will destroy

**C.** $t_{rr}$ is depends on softness factor

**D.** schottky diodes have low $t_{rr}$

**Options:**

(i) All are true

(ii) A, B, D

**(iii) A, B,C**

(iv) B,C, D

The feature of schottky diode is low forward voltage drop, not low $t_{rr.}$

**[**39**]** The MOSFET has

(i)Higher Power handling capability than BJT

(ii) Faster switching speed than BJT

(iii) High on state resistance

(iv) Secondary breakdown voltage problem

which of the above statements are incorrect?

**Options:**

**A. (i), (iii), (iv)**

**B.** (ii), (iii)

**C.** All of the above

**D.** (ii), (iii), (iv)

**[**40**]** Which of the following is called as uncontrolled semiconductor device?

**A. Diode**

**B.** Thyristor

**C.** GTO

**D.** MOSFET

**[**41**]** Which of the following is a half controlled semiconductor device?

**A.** MOSFET

**B.** GTO

**C.** MCT

**D. SCR**

**HINT:-**In SCR only turn on of the device an be controllable by the gate signal.

**[**42**]**Which of the following abbreviation is not a power semiconductor device?

**A.** SIT

**B.** SITH

**C.** MCT

**D.** IGCT

**Options:**

1. a and d
2. a only
3. a, b, d
4. **All are power semiconductor device**

**HINT:-** SIT – Static Induction Transistor
SITH – Static Induction Thyristor
MCT - MOS Controlled Thyristor
IGCT – Integrated Gate Commutated Thyristor

**[**43**]** Which of the following statements are correct?

**A.** IGBT is current driven device
**B.** IGCT is voltage driven device
**C.** MOSFET is voltage driven device
**D.** GTO is minority carrier device

**Options:**

1. a, b, c
**2. b, c, d**
3. All are correct
4. None are correct

**[**44**]** The breakdown mechanism in a lightly doped p-n junction under reverse biased condition is called

**A. avalanche breakdown**
**B.** zener breakdown
**C.** breakdown by tunnelling
**D.** high voltage breakdown

**[**45**]** For a large values of |VDS|, a FET behave as

**A.** Voltage controlled resistor
**B.** Current controlled current source
**C. Voltage controlled current source**
**D.** Current controlled resistor

**[**46**]** In a full wave rectifier without filter, the ripple factor is

**A. 0.482**
**B.** 1.21
**C.** 1.79
**D.** 2.05

**[**47**]** Space charge region around a P-N junction

**A. does not contain mobile carries**
**B.** contains both free electrons and holes
**C.** contains one type of mobile carriers depending on the level of doping of the P or N regions
**D.** contains electrons only as free carriers

**[**48**]** In a JFET, at pinch-off voltage applied on the gate

**A.** The drain current becomes almost zero
**B.** The drain current begins to decrease
**C. The drain current is almost at saturation value**
**D.** The drain to source voltage is close to zero volts

**[**49**]** The value of ripple factor of a half wave rectifier without filter is approximately

**A. 1.2**
**B.** o.2
**C.** 2.2
**D.** 2.0

**[**50**]** In an intrinsic semiconductor, the Fermi-level is

**A.** closer to the valence band
**B.** midway between conduction and valence band
**C. closer to the conduction band**
**D.** within the valence band

**[**51**]** The transformer utilization factor of a half wave rectifier is approximately

**A.** 0.6
**B. 0.3**
**C.** 0.9

**D.** 1.1

**[**52**]** Transistor is a

**A. Current controlled current device**

**B.** Current controlled voltage device

**C.** Voltage controlled current device

**D.** Voltage controlled voltage device

**HINT:-** For ex, the output current Ic depends on the input current Ib

**[**53**]** If the output voltage of a bridge rectifier is 100V, the PIV of diode will be

**A.** 100 * Square root(2) V

**B.** 200/(pi) V

**C.** 100 * (pi) V

**D. 100/2 V**

**HINT:-**Peak inverse voltage = max secondary voltage = Vdc= 2Vm/pi = 100

Vm = 100 * pi/2

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= 3.69 * √**[**(180 -45)/180**]**

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Iav = Vav/R = 12/24 = 0.5A

Vrms= V* Square root (Ton) * f = 48 * Square root (0.25) = 24V

Irms = Vrms/R = 24/24 = 1A

P = Irms * Irms * R = 1 * 24 = 24W

.....

**[**56**]** A thyristor half wave controlled converter has a supply voltage of 240V at 50Hz and a load resistance of 100 Ohm. when the firing delay angle is 30 the average value of load current is

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**Exp:**

Vav = **[**2Vm/(π)**]**cosα**]**
= **[**(2 *√(2*110)/ 3.14 **]** * cos 75
= 99 cos 75
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Iav = Vav / R
= 25.6/55
= 0.446A = Irms
P = Irms * Irms * R
= 0.446 * 0.446 * 55
=10.9W

.....

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Iav = Vav/R = 152.6 / 50 = 3.05A = Irms
P = Square of Irms * R = 3.04 * 3.04 * 50 = 466W

**[**60**]** The reverse recovery time of the diode is defined as the time between the instant diode current becomes zero and the instant reverse recovery current decays to

**A.** Zero
**B.** 10% of the reverse peak current (IRM)

**C. 25% of (IRM)**

**D.** 15% of (IRM)

**[**61**]** The cut-in voltage and forward-voltage drop of the diode are respectively

**A.** 0.7V, 0.7V

**B.** 0.7V, 1V

**C. 0.7V, 0.6V**

**D.** 1V, 0.7V

**[**62**]** The softness factor for soft-recovery and fast-recovery diodes are respectively

**A.** 1, >1

**B.** <1, 1

**C.** 1, 1

**D. 1, <1**

**[**63**]** Reverse recovery current in a diode depends on

**A. Forward field current**

**B.** Storage charge

**C.** Temperature

**D.** PIV

**[**64**]** The three terminals of power MOSFET

**A.** Collector, Emitter, base

**B.** Drain, source, base

**C. Drain, source, gate**

**D.** Collector, emitter, gate

**[**65**]**The three terminals of IGBT

**A.** Collector, emitter, base

**B.** Drain, source, base

**C.** Drain, source, gate

**D. Collector, emitter, gate**

**[**66**]** The three terminals of MCT

**A. Anode, cathode, gate**

**B.** Collector, emitter, gate

**C.** Drain, source, base

**D.** Drain, source, gate

**[**67**]** Compared to Power MOSFET, the Power BJT has

**A.** Lower switching losses but higher conduction loss

**B.** Higher switching losses and higher conduction loss

**C. Higher switching losses but lower conduction loss**

**D.** Lower switching losses and lower conduction loss

**[**68**]** Which one of the following statement is true

**A. MOSFET has positive temperature coefficient whereas BJT has negative temperature Coefficient**

**B.** Both MOSFET and BJT have positive temperature coefficient

**C.** Both MOSFET and BJT have negative temperature coefficient

**D.** MOSFET has negative temperature coefficient whereas BJT has positive temperature coefficient

**[**69**]** Which one of the following statement is true?

**A.** Both MOSFET and BJT are voltage controlled devices

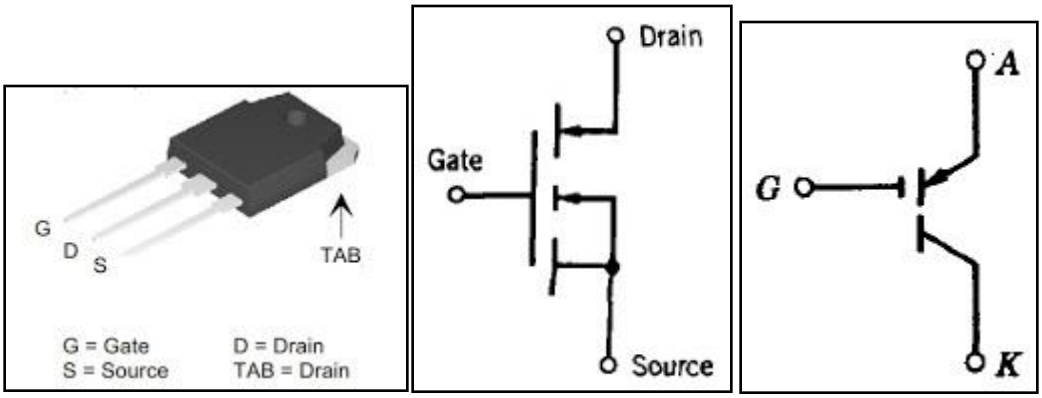
**B.** Both MOSFET and BJT are current controlled devices

**C. MOSFET is a voltage controlled device and BJT is current controlled device**

**D.** MOSFET is a current controlled device and BJT is voltage controlled device

**HINT:-**MOSFET operation is controlled by gate voltage and the BJT operation is controlled by base current

**HINT for Questions 5, 6, 7:**

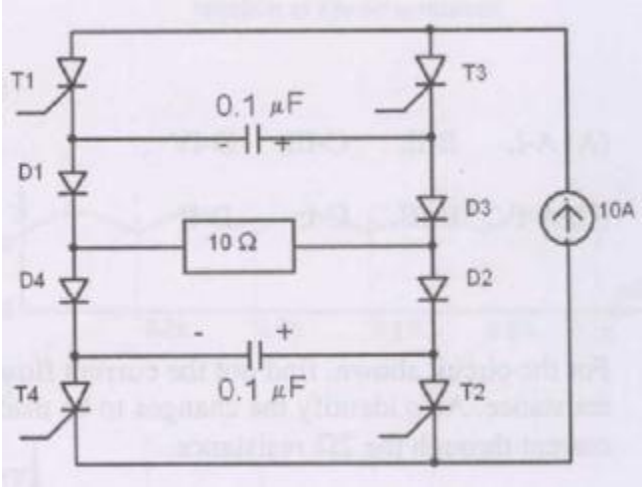



**MOSFET** **IGBT** **MCT**

**[**70**]**An SCR is considered to be a semi-controlled device because **[**GATE 2009**]**

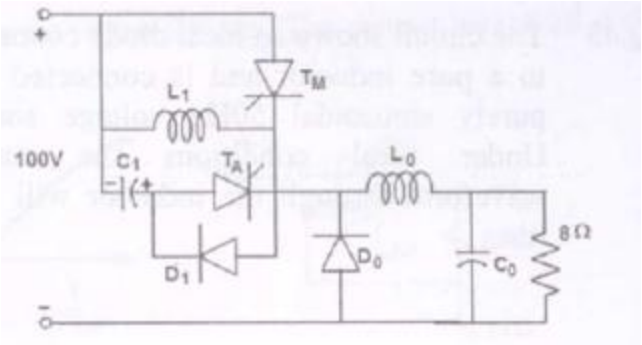
**A.** It can be turned OFF but not ON with a gate pule
**B.** It conducts only during one half-cycle of an alternating current wave
**C. It can be turned ON but not OFF with a gate pulse**
**D.** It can be turned ON only during one half-cycle of an alternating voltage wave

**[**71**]** The current Source Inverter shown in figure is operated by alternatively turning on thyristor pairs($T_1$,$T_2$) and ($T_3$,$T_4$). If the load is purely resistive, the theoretical maximum output frequency obtainable will be **[**GATE**]**



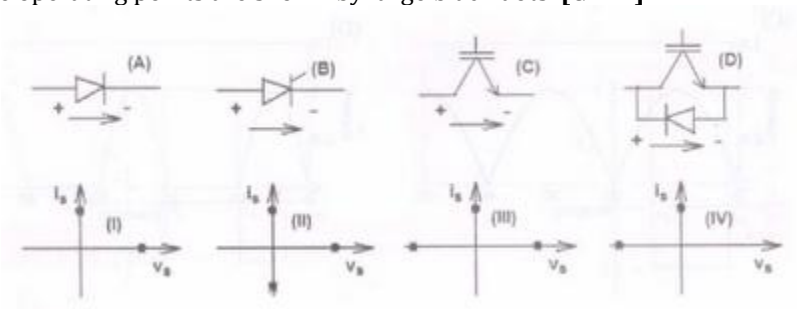

**A.** 125kHz
**B.** 250kHz
**C. 500kHz**
**D.** 50kHz

**[**72**]** In the chopper circuit shown, the main thyristor($T_M$) is operated at a duty ratio of 0.8 which is much larger the communication interval. If the maximum allowable reapplied dv/dt on $T_M$ is 50V/μs,what should be the theoretical minimum value of $C_1$? Assume current ripple through $L_0$ to be negligible. **[**GATE**]**




**A. 0.2μF**
**B.** 0.02μF
**C.** 2μF
**D.** 20μF

**[**73**]** Match the switch arrangements on the top row to the steady-state V-I characteristics on the lower row.The steady state operating points are shown by large black dots. **[**GATE**]**




**A.** A-I, B-II, C-III, D-IV
**B.** A-II, B-IV, C-I, D-III
**C. A-I, B-II, C-III, D-II**
**D.** A-IV, B-III, C-II, D-I

**[**74**]** " Six MOSFETs connected in a bridge configuration (having no other power device) MUST be operated as a Voltage Source Inverter (VSI) ". This statement is **[**GATE 2007**]**

**A.** True, because being majority carrier devices, MOSFETs are voltage driven
**B.** True, because MOSFETs have inherently anti parallel diodes
**C.** False, because it can be operated both as current source Inverter (CSI) or a VSI
**D. False, because MOSFETs can be operated as excellent constant current sources in the saturation region**

**[**75**]** A single phase full - wave half controlled bridge converter feeds an inductive loa**D.** The two SCRs in the converter are connected to a common DC bus. The converter has to have a free wheeling diode **[**GATE 2007**]**

**A.** Because the converter inherently does not provide for free wheeling
**B. Because the converter does not provide for free wheeling for high values of triggering angles**
**C.** Or else the free wheeling action of the converter will cause shorting of the AC supply
**D.** Or else if a gate pulse to one of the SCRs is missed, it will subsequently cause a high load current in the other SCR

**[**76**]** A single phase fully controlled thyristor bridge ac-dc converter is operating at a firing angle of 25 degree, and an overlap angle 10 degree with constant dc output current of 20**A.** The fundamental power factor ( displacement factor) at input ac mains is **[**GATE 2007**]**

**A. 0.78**
**B.** 0.827
**C.** 0.866
**D.** 0.9

**[**77**]** A three phase fully controlled thyristor bridge converter is used as line commutated inverter to feed 50KW power at 420V DC to a three phase 415V(line), 50Hz as mains. Consider Dc link current to be constant. The rms current of the thyristor is **[**GATE 2007**]**

**A.** 119.05A
**B.** 79.37A
**C.** 68.73A
**D. 39.68A**

**Statement for Linked Answer Questions:78 & 79 [GATE2012]**

The transfer function of a compensator is given as GC(s)=**[**(s+a)/(s+b)**]**

**[**78**]** $G_C(s)$ is a lead compensator if

**A. a=1,b=2**
**B.** a=3,b=2
**C.** a=-3,b=-1
**D.** a=3,b=1

**[**79**]** The phase of the above lead compensator is maximum at

**A. $\sqrt{2}$ rad/s**
**B.** $\sqrt{3}$ rad/s
**C.** $\sqrt{6}$ rad/s
**D.** $\sqrt{1/3}$ rad/s

**[**80**]** Which of the following statements are correct?

1. Thyristor is current driven device
2. GTO is current driven device
3. GTR is current driven device
4. SCR is a pulse triggered device

**A.**1 and 2
**B.**1, 2, 3
**C.All**
**D.**4 only

**[**81**]** Which of the following statements are correct?

1.GTO is a pulse triggered device
2.MOSFET is uni-polar device
3.SCR is a bipolar device
4.Continuous gate signal is not required to maintain the SCR to be in ON state

**A.** 1, 2, 4 only
**B.** 1, 2 only
**C.** 4 only
**D. All**

**[**82**]** Which of the following is not a fully controlled semiconductor device?

**A.** MOSFET
**B.** IGBT
**C.** IGCT
**D. SCR**
**HINT:-Only turn on of the SCR can be controlled whereas in other devices we can control both turn on and turn off**

**[**83**]** Which of the following is not associated with p-n junction

**A.** junction capacitance
**B.** charge storage capacitance
**C.** depletion capacitance
**D. channel length modulation**

**[**84**]** In a p-n junction diode under reverse bias, the magnitude of electric field is maximum at

**A.** the edge of the depletion region on the p-side
**B.** the edge of the depletion region on the n-side
**C. the p-n junction**
**D.** the center of the depletion region on the n-side

**[**85**]** An n-channel JFET has IDSS=2mA, and Vp=-4V. Its transconductance gm=(in mA/V) for an applied gate to source voltage VGS=-2V is

**A.** 0.25
**B. 0.5**
**C.** 0.75
**D.** 1

**[**86**]**The MOSFET switch in its on-state may be considered equivalent to

**A.** resistor
**B.** inductor
**C. capacitor**
**D.** battery

**[**87**]** The effective channel length of a MOSFET in a saturation decreases with increase in

**A.** gate voltage
**B. drain voltage**
**C.** source voltage
**D.** body voltage

**[**88**]** The early effect in a bipolar junction transistor is caused by

**A.** Fast turn – on
**B.** Fast turn – off
**C. Large collector - base reverse bias**
**D.** Large emmiter - base forward bias

**[**89**]** MOSFET can be used as a

**A.** Current controlled capacitor
**B. Voltage controlled capacitor**
**C.** Current controlled inductor
**D.** Voltage controlled inductors