

Chapter 7

Principles of Compiler Design

In this chapter,

CFG stands for context free grammar.

DFSA stands for deterministic finite state automata.

NDFSA stands for non-deterministic finite state automata.

1. Cross-compiler is a compiler
 - (a) which is written in a language that is different from the source language.
 - (b) that generates object code for its host machine.
 - (c) which is written in a language that is same as the source language.
 - (d) that runs on one machine but produces object code for another machine.
2. Incremental-compiler is a compiler
 - (a) which is written in a language that is different from the source language
 - (b) that generates object code for its host machine
 - (c) which is written in a language that is same as the source language
 - (d) that allows a modified portion of a program to be recompiled
3. For which of the following reasons, an interpreter is preferred to a compiler?
 - (a) It takes less time to execute.
 - (b) It is much helpful in the initial stages of program development.
 - (c) Debugging can be faster and easier.
 - (d) It needs less computer resources.

4. For which of the following reasons, a compiler is preferable to an interpreter?
 - (a) It can generate stand-alone programs that often take less time for execution.
 - (b) It is much helpful in the initial stages of program development.
 - (c) Debugging can be faster and easier.
 - (d) If one changes a statement, only that statement needs recompilation.
5. The cost of developing a compiler is proportional to the
 - (a) complexity of the source language
 - (b) complexity of the architecture of the target machine
 - (c) flexibility of the available instruction set
 - (d) none of the above
6. An ideal compiler should
 - (a) be smaller in size
 - (b) take less time for compilation
 - (c) be written in a high level language
 - (d) produce object code that is smaller in size and executes faster
7. An optimizing compiler
 - (a) is optimized to occupy less space
 - (b) is optimized to take less time for execution
 - (c) optimizes the code
 - (d) none of the above
8. In a compiler, grouping of characters into tokens is done by the
 - (a) scanner
 - (b) parser
 - (c) code generator
 - (d) code optimizer
9. Whether a given pattern constitutes a token or not
 - (a) depends on the source language
 - (b) depends on the target language
 - (c) depends on the compiler
 - (d) none of the above comments is true
10. A grammar will be meaningless if the
 - (a) terminal set and the non-terminal set are not disjoint
 - (b) left hand side of a production is a single terminal
 - (c) left hand side of a production has no non-terminal
 - (d) left hand side of a production has more than two non-terminals
11. Which of the following grammars are not phase-structured?
 - (a) Regular
 - (b) Context-free
 - (c) Context-sensitive
 - (d) None of the above
12. Which of the following is the most general phase-structured grammar?
 - (a) Regular
 - (b) Context-free
 - (c) Context-sensitive
 - (d) None of the above
13. In a context-sensitive grammar,
 - (a) ϵ can't be the right hand side of any production
 - (b) number of grammar symbols on the left hand side of a production can't be greater than the number of grammar symbols on the right hand side

- (c) number of grammar symbols on the left hand side of a production can't be greater than the number of terminals on the right hand side
- (d) number of grammar symbols on the left hand side of a production can't be greater than the number of non-terminals on the right hand side
14. In a context-free grammar,
- (a) ϵ can't be the right hand side of any production
- (b) terminal symbols can't be present in the left hand side of any production
- (c) the number of grammar symbols in the left hand side is not greater than the number of grammar symbols in the right hand side
- (d) all of the above
15. If w is a string of terminals and A, B are two non-terminals, then which of the following are right-linear grammars?
- (a) $A \rightarrow Bw$ (b) $A \rightarrow Bw|w$ (c) $A \rightarrow wB|w$ (d) None of the above
16. If a is a terminal and S, A, B are three non-terminals, then which of the following are regular grammars?
- (a) $S \rightarrow \epsilon$ (b) $A \rightarrow aB|a$
 $A \rightarrow aS|b$ $B \rightarrow bA|b$
- (c) $A \rightarrow Ba|Bab$ (d) $A \rightarrow abB|aB$
17. Representing the syntax by a grammar is advantageous because
- (a) it is concise
- (b) it is accurate
- (c) automation becomes easy
- (d) intermediate code can be generated easily and efficiently
18. CFG can be recognized by a
- (a) push-down automata (b) 2-way linear bounded automata
- (c) finite state automata (d) none of the above
19. CSG can be recognized by
- (a) push-down automata (b) 2-way linear bounded automata
- (c) finite state automata (d) none of the above
20. Choose the correct statements.
- (a) Sentence of a grammar is a sentential form without any terminals.
- (b) Sentence of a grammar should be derivable from the start state.
- (c) Sentence of a grammar should be frontier of a derivation tree, in which the root node has the start state as the label.
- (d) All of the above
21. A grammar can have
- (a) a non-terminal A that can't derive any string of terminals
- (b) a non-terminal A that can be present in any sentential form
- (c) ϵ as the only symbol on the left hand side of a production
- (d) none of the above

22. A top-down parser generates
- (a) left-most derivation
 - (b) right-most derivation
 - (c) right-most derivation in reverse
 - (d) left-most derivation in reverse
23. A bottom-up parser generates
- (a) left-most derivation
 - (b) right-most derivation
 - (c) right-most derivation in reverse
 - (d) left-most derivation in reverse
24. A given grammar is said to be ambiguous if
- (a) two or more productions have the same non-terminal on the left hand side
 - (b) a derivation tree has more than one associated sentence
 - (c) there is a sentence with more than one derivation tree corresponding to it
 - (d) parenthesis are not present in the grammar
- *25. The grammar $E \rightarrow E+E \mid E * E \mid a$, is
- (a) ambiguous
 - (b) unambiguous
 - (c) ambiguous or not depends on the given sentence
 - (d) none of the above
26. Choose the correct statement.
- (a) Language corresponding to a given grammar, is the set of all strings that can be generated by the given grammar.
 - (b) A given language is ambiguous if no unambiguous grammar exists for it.
 - (c) Two different grammars may generate the same language.
 - (d) None of the above
- *27. Consider the grammar
- $$S \rightarrow ABSc \mid A^nb^nc$$
- $$BA \rightarrow AB$$
- $$Bb \rightarrow bb$$
- $$Ab \rightarrow ab$$
- $$Aa \rightarrow aa$$
- Which of the following sentences can be derived by this grammar?
- (a) abc
 - (b) aab
 - (c) abcc
 - (d) abbc
- *28. The language generated by the above grammar is the set of all strings, made up of a, b, c, such that
- (a) the number of a's, b's, and c's will be equal
 - (b) a's always precede b's
 - (c) b's always precede c's
 - (d) the number of a's b's and c's are same and the a's precede b's, which precede c's.
29. In an incompletely specified automata
- (a) no edge should be labeled ϵ
 - (b) from any given state, there can't be any token leading to two different states

- (c) some states have no transition on some tokens
 - (d) start state may not be there
30. The main difference between a DFSA and an NDFSA is
- (a) in DFSA, ϵ transition may be present
 - (b) in NDFSA, ϵ transitions may be present
 - (c) in DFSA, from any given state, there can't be any alphabet leading to two different states.
 - (d) in NDFSA, from any given state, there can't be any alphabet leading to two different states.
31. Two finite state machines are said to be equivalent if they
- (a) have the same number of states
 - (b) have the same number of edges
 - (c) have the same number of states and edges
 - (d) recognize the same set of tokens
32. Choose the correct answer.
FORTRAN is a
- (a) regular language
 - (b) context-free language
 - (c) context-sensitive language
 - (d) Turing language
33. If two finite states machine M and N are isomorphic, then M can be transformed to N by re-labeling
- (a) the states alone
 - (b) the edges alone
 - (c) both the states and edges
 - (d) none of the above
34. In a syntax directed translation scheme, if the value of an attribute of a node is a function of the values of the attributes of its children, then it is called a
- (a) synthesized attribute
 - (b) inherited attribute
 - (c) canonical attribute
 - (d) none of the above
35. Synthesized attribute can easily be simulated by an
- (a) LL grammar
 - (b) ambiguous grammar
 - (c) LR grammar
 - (d) none of the above
36. For which of the following situations, inherited attribute is a natural choice?
- (a) Evaluation of arithmetic expressions
 - (b) Keeping track of variable declaration
 - (c) Checking for the correct use of L-values and R-values
 - (d) All of the above
37. The graph depicting the inter-dependencies of the attributes of different nodes in a parse tree is called a
- (a) flow graph
 - (b) dependency graph
 - (c) Karnaugh's graph
 - (d) Steffi graph

38. Choose the correct statements.
- (a) Topological sort can be used to obtain an evaluation order of a dependency graph.
 - (b) Evaluation order for a dependency graph dictates the order in which the semantic rules are done.
 - (c) Code generation depends on the order in which the semantic actions are performed.
 - (d) Only (a) and (c) are correct.
39. A syntax tree
- (a) is another name for a parse tree
 - (b) is a condensed form of parse tree
 - (c) should not have keywords as leaves
 - (d) none of the above
40. Syntax directed translation scheme is desirable because
- (a) it is based on the syntax
 - (b) its description is independent of any implementation
 - (c) it is easy to modify
 - (d) only (a) and (c) are correct
41. Which of the following is not an intermediate code form?
- (a) Postfix notation
 - (b) Syntax trees
 - (c) Three address codes
 - (d) Quadruples
42. Three address codes can be implemented by
- (a) indirect triples
 - (b) direct triples
 - (c) quadruples
 - (d) none of the above
43. Three address code involves
- (a) exactly 3 addresses
 - (b) at the most 3 addresses
 - (c) no unary operator
 - (d) none of the above
44. Symbol table can be used for
- (a) checking type compatibility
 - (b) suppressing duplicate error messages
 - (c) storage allocation
 - (d) none of the above
45. The best way to compare the different implementations of symbol table is to compare the time required to
- (a) add a new name
 - (b) make an inquiry
 - (c) add a new name and make an inquiry
 - (d) none of the above
46. Which of the following symbol table implementation is based on the property of locality of reference?
- (a) Linear list
 - (b) Search tree
 - (c) Hash table
 - (d) Self-organization list
- *47. Which of the following symbol table implementation is best suited if access time is to be minimum?
- (a) Linear list
 - (b) Search tree
 - (c) Hash table
 - (d) Self organization list
48. Which of the following symbol table implementation, makes efficient use of memory?
- (a) List
 - (b) Search tree
 - (c) Hash table
 - (d) Self-organizing list

49. Access time of the symbol table will be logarithmic, if it is implemented by a
(a) linear list (b) search tree (c) hash table (d) self-organizing list
50. An ideal compiler should
(a) detect error (b) detect and report error
(c) detect, report and correct error (d) none of the above
51. Which of the following is not a source of error?
(a) Faulty design specification (b) Faulty algorithm
(c) Compiler themselves (d) None of the above
52. Any transcription error can be repaired by
(a) insertion alone (b) deletion alone
(c) insertion and deletion alone (d) replacement alone
53. Hamming distance is a
(a) theoretical way of measuring errors
(b) technique for assigning codes to a set of items known to occur with a given probability
(c) technique for optimizing the intermediate code
(d) none of the above
54. Error repair may
(a) increase the number of errors (b) generate spurious error messages
(c) mask subsequent errors (d) none of the above
55. A parser with the valid prefix property is advantageous because
(a) it detects error as soon as possible
(b) it detects errors as and when they occur
(c) it limits the amount of erroneous output passed to the next phase
(d) all of the above
56. The advantage of panic mode of error recovery is that
(a) it is simple to implement (b) it is very effective
(c) it never gets into an infinite loop (d) none of the above
57. To recover from an error, the operator precedence parser may
(a) insert symbols onto the stack (b) insert symbols onto the input
(c) delete symbols from the stack (d) delete symbols from the input
58. Which of the following optimization techniques are typically applied on loops?
(a) Removal of invariant computation (b) Elimination of induction variables
(c) Peephole optimization (d) Constant folding
59. The technique of replacing run time computations by compile time computations is called
(a) constant folding (b) code hoisting
(c) peephole optimization (d) invariant computation
60. The graph that shows the basic blocks and their successor relationship is called
(a) control graph (b) flow graph (c) DAG (d) Hamiltonian graph

61. Reduction in strength means
- (a) replacing run time computation by compile time computation
 - (b) removing loop invariant computation
 - (c) removing common sub-expressions
 - (d) replacing a costly operation by a relatively cheaper one
62. A basic block can be analyzed by a
- (a) DAG
 - (b) graph which may involve cycles
 - (c) flow-graph
 - (d) none of the above
63. *ud*-chaining is useful for
- (a) determining whether a particular definition is used anywhere or not
 - (b) constant folding
 - (c) checking whether a variable is used, without prior assignment
 - (d) none of the above
64. Which of the following concepts can be used to identify loops?
- (a) Dominators
 - (b) Reducible graphs
 - (c) Depth first ordering
 - (d) None of the above
65. Which of the following are not loop optimization techniques?
- (a) Jamming
 - (b) Unrolling
 - (c) Induction variable elimination
 - (d) None of the above
66. Running time of a program depends on the
- (a) way the registers are used
 - (b) order in which computations are performed
 - (c) way the addressing modes are used
 - (d) usage of machine idioms
67. *du*-chaining
- (a) stands for use definition chaining
 - (b) is useful for copy propagation removal
 - (c) is useful for induction variable removal
 - (d) none of the above
68. Which of the following comments about peep-hole optimization are true?
- (a) It is applied to a small part of the code.
 - (b) It can be used to optimize intermediate code.
 - (c) To get the best out of this technique, it has to be applied repeatedly.
 - (d) It can be applied to a portion of the code that is not contiguous.
- *69. Shift-reduce parsers are
- (a) top-down parsers
 - (b) bottom-up parsers
 - (c) may be top-down or bottom-up parsers
 - (d) none of the above

80. Consider an ϵ -free CFG. If for every pair of productions $A \rightarrow u$ and $A \rightarrow v$
- if $FIRST(u) \cap FIRST(v)$ is empty then the CFG has to be LL(1)
 - if the CFG is LL(1) then $FIRST(u) \cap FIRST(v)$ has to be empty
 - if $FIRST(u) \cap FIRST(v)$ is empty then the CFG cannot be LL(1)
 - none of the above
81. LR(k) grammar
- can only examine a maximum of k input symbols
 - can be used to identify handles
 - can be used to identify the production associated with a handle
 - covers the LL(k) class
82. The set of all viable prefixes of right sentential form of a given grammar
- can be recognized by a finite state machine
 - cannot be recognized by a finite state machine
 - can be used to control an LR(k) parser
 - none of the above
83. The 'k', in LR (k) cannot be
- 0
 - 1
 - 2
 - none of the above

The next three questions are based on the following grammar

$$\begin{aligned} E &\rightarrow E/X \mid X \\ X &\rightarrow T-X \mid X*T \mid T \\ T &\rightarrow T+F \mid F \\ F &\rightarrow (E) \mid id \end{aligned}$$

(id stands for identifier)

84. This grammar is
- unambiguous
 - ambiguous
 - context-free
 - none of these
85. The above grammar is used to generate all valid arithmetic expressions in a hypothetical language in which
- / associates from the left
 - associates from the left
 - + associative from the left
 - * associative from the left
86. The above grammar is used to generate all valid arithmetic expressions in a hypothetical language in which
- + has the highest precedence
 - * has the highest precedence
 - has the highest precedence
 - / has the highest precedence
87. Back-patching is useful for handling
- conditional jumps
 - unconditional jumps
 - backward references
 - forward references

Let x be a string and let A be a non-terminal. $FIRST_k(x)$ is the set of all leading terminal strings of length k or less, in the strings derivable from x .

$FOLLOW_k(A)$ is the set of all derivable terminal strings of length k or less, that can follow A in some left-most sentential form.

The next three questions are based on the above definition.

88. Consider the grammar

$$E \rightarrow TE'$$

$$E' \rightarrow +TE' \mid \epsilon$$

$$T \rightarrow FT'$$

$$T' \rightarrow *FT' \mid \epsilon$$

$$F \rightarrow (E) \mid id$$

$FIRST_1(E)$ will be same as that of

- (a) $FIRST_1(T)$ (b) $FIRST_1(F)$ (c) $FIRST_1(T')$ (d) all of the above

89. $FOLLOW_1(F)$ is

- (a) $\{+, *,), \$\}$ (b) $\{+,), \$\}$
 (c) $\{*,), \$\}$ (d) $\{+, (,), *\}$

90. Which of the following remarks logically follows?

- (a) $FIRST_k(\epsilon) = \{\epsilon\}$
 (b) If $FOLLOW_k(A)$ contains ϵ , then A is the start symbol
 (c) If $A \rightarrow w$, is a production in the given grammar G , then $FIRST_k(A)$ contains $FIRST_k(w)$
 (d) If $A \rightarrow w$, is a production in the given grammar G , then $FIRST_k(w)$ contains $FIRST_k(A)$

91. Merging states with a common core may produce _____ conflicts but does not produce _____ conflicts in an LALR parser

- (a) reduce–reduce; shift–reduce (b) shift–reduce; reduce–reduce
 (c) shift–reduce; shift–reduce (d) none of the above

92. For a CFG, $FOLLOW(A)$ is the set of all terminals that can immediately appear to the right of the non-terminal A in some sentential form. We define two sets $LFOLLOW(A)$ and $RFOLLOW(A)$ by replacing the word sentential by “Left most sentential” and “Right most sentential” respectively in the definition of $FOLLOW(A)$.

Choose the correct statement(s).

- (a) $FOLLOW(A)$ and $LFOLLOW(A)$ may be different
 (b) $FOLLOW(A)$ and $RFOLLOW(A)$ are always the same
 (c) All the three are same
 (d) All the three are different

93. In a programming language, an identifier is permitted to be a letter followed by any number of letters or digits. If L and D denote the set of letters and digits respectively, which of the following expressions defines an identifier?

- (a) $(L \cup D)^+$ (b) $L.(L \cup D)^*$ (c) $(L.D)^*$ (d) $L.(L.D)^*$

Explanations

25. Consider the string $a+a*a$. It can be derived as

$$E \rightarrow E+E \rightarrow E+E*E \rightarrow a+E*E \rightarrow a+a*E \rightarrow a+a*a$$

or

$$E \rightarrow E*E \rightarrow E+E*E \rightarrow a+E*E \rightarrow a+a*E \rightarrow a+a*a$$

Since we know a string that can be derived in more than one way, the given grammar is ambiguous.

27. abc can be derived as follows.

$$S \rightarrow Abc \rightarrow abc \text{ using } (Ab \rightarrow ab)$$

As we see, any production from the start state has to end in c . So aab is impossible. Options (c) and (d) are also not possible.

28. Generate some of the strings that can be derived from the start state and verify that they fall into the category covered by option (d).
47. If memory space is not the constraint, then by increasing the number of bins to K , the access time can be reduced by a factor of K . So, average number of items in a bin will decrease as the number of bins increases. In the case of list, access time will be proportional to n , the number of items, but we will be using as much memory space as is absolutely necessary. In the case of search tree implementation, the access time will be logarithmic.
69. Any shift-reduce parser typically works by shifting entries onto the stack. If a handle is found on the top of the stack, it is popped and replaced by the corresponding left hand side of the production. If ultimately we have only the starting non-terminal on the stack, when there are no more tokens to be scanned, the parsing will be successful. So, it is bottom-up.
94. The right-most derivation of the string $xxxxxyzz$ is,

$$S \rightarrow xxW \rightarrow xxSz \rightarrow xxxxWz \rightarrow xxxxSzz \rightarrow xxxxyzz.$$
 A shift reduce parser, performs the right-most derivation in reverse. So, first it reduces the y to s , by the production $S \rightarrow y$. As a consequence of this, 2 is immediately printed. Next, Sz is reduced to W , by the production $W \rightarrow Sz$. So, 3 will be printed. Proceeding this way, we get the output string 23131.
95. It is because, it is equivalent to recognizing wcw , where the first w is the declaration and the second is its use. wcw is not a CFG.

- *8. If X , Y and Z are 3 Boolean variables, then $X(Y + Z)$ equals $(X + Y)(X + Z)$, if X , Y , Z take the values
 (a) 1, 0, 0 (b) 0, 1, 0 (c) 1, 1, 0 (d) 0, 1, 1
- *9. Which of the following comments about the Program Counter (PC) are true?
 (a) It is a register.
 (b) It is a cell in ROM.
 (c) During execution of the current instruction, its content changes.
 (d) None of the above.
- *10. If $(123)_5 = (A3)_B$, then the number of possible values of A is
 (a) 4 (b) 1 (c) 3 (d) 2
11. The speed imbalance between memory access and CPU operation can be reduced by
 (a) cache memory (b) memory interleaving
 (c) reducing the size of memory (d) none of the above
- *12. If $(12A)_3 = (123)_A$, then the value of A is
 (a) 3 (b) 3 or 4 (c) 2 (d) none of the above
- *13. Choose the correct statements.
 (a) By scanning a bit pattern, one can say whether, it represents data or not.
 (b) Whether a given piece of information is a data or not depends on the particular application.
 (c) Positive numbers can't be represented in 2's complement form.
 (d) Positive numbers can't be represented in 1's complement form.
14. Which of the following does not need extra hardware for DRAM refreshing?
 (a) 8085 (b) Motorola-6800 (c) Z-80 (d) None of the above
15. The advantage of MOS devices over bipolar devices is
 (a) it allows higher bit densities and also cost effective
 (b) it is easy to fabricate
 (c) its higher-impedance
 (d) its operational speed
- *16. The Boolean expression $X + X'Y$ equals
 (a) $X + Y$ (b) $X + XY$ (c) $Y + YX$ (d) $X'Y + Y'X$
- *17. $(X + Y) + Z = X + (Y + Z)$
 (a) shows that the Boolean operator OR is distributive
 (b) shows that the Boolean operator OR is associative
 (c) implies the associativity of the Boolean operator AND
 (d) none of the above
18. Which of the following are registers?
 (a) Accumulator (b) Stack pointer (c) Program counter (d) Buffer

19. Which of the following remarks about BCD are true?
- (a) It is a 8-4-2-1 weighted code
 - (b) Complement of a number can be found efficiently
 - (c) $(12345678)_{10}$ needs 4 bytes in BCD representation
 - (d) Conversion to and from the decimal system can be done easily
20. The first operating system used in microprocessors is
- (a) Zenix
 - (b) DOS
 - (c) CP/M
 - (d) Multics
21. Which of the following remarks about PLA is/are true?
- (a) It produces product of sum as the output.
 - (b) It produces sum of products as the output.
 - (c) It is dedicated for a particular operation.
 - (d) It is general.
- *22. Any given truth table can be represented by a
- (a) Karnaugh map
 - (b) sum of product of Boolean expressions
 - (c) product of sum of Boolean expressions
 - (d) none of the above
- *23. A number system uses 20 as the radix. The excess code that is necessary for its equivalent binary coded representation is
- (a) 4
 - (b) 5
 - (c) 6
 - (d) 7
24. Choose the correct statements.
- (a) Bus is a group of information carrying wires.
 - (b) Bus is needed to achieve reasonable speed of operation.
 - (c) Bus can carry data or address.
 - (d) A bus can be shared by more than one device.
- *25. $A+B$ can be implemented by
- (a) NAND gates alone
 - (b) NOR gates alone
 - (c) AND gates alone
 - (d) none of the above
26. Bipolar devices are desirable in the fabrication of which of the following components?
- (a) Main memory
 - (b) Cache memory
 - (c) Micro program memory
 - (d) All of the above
27. Which of the following is the programmable internal timer?
- (a) 8251
 - (b) 8250
 - (c) 8253
 - (d) 8275
- *28. The idea of cache memory is based on the
- (a) property of locality of reference
 - (b) fact that only a small portion of a program is referenced relatively frequently
 - (c) heuristic 90-10 rule
 - (d) fact that references generally tend to cluster

- *29. Which of the following weights makes the complement operation easier in BCD form?
(a) 8-4-2-1 (b) Excess-3 (c) 2-4-2-1 (d) 3-2-1-0
30. The sequence of events that happen during a typical fetch operation is
(a) PC → Mar → Memory → MDR → IR (b) PC → Memory → MDR → IR
(c) PC → Memory → IR (d) PC → MAR → Memory → IR
- *31. Any given Boolean expression can be implemented by using
(a) only NAND gates (b) only NOR gates
(c) only OR gates (d) only AND gates
- *32. To get Boolean expression in the product of sum form, from a given Karnaugh map
(a) don't care conditions should not be present
(b) don't care conditions, if present, should be taken as zeroes
(c) one should cover all the 0's present and complement the resulting expression
(d) one should cover all the 1's present and complement the resulting expression
- *33. The Boolean expression $AB + AB' + A'C + AC$ is unaffected by the value of the Boolean variable
(a) A (b) B (c) C (d) none of the above
- *34. The minimum number of gates required to implement the Boolean expression $AB + AB' + A'C$ is
(a) 1 AND gate and 1 OR gate (b) 2 NAND gates
(c) 3 AND gates and 2 OR gates (d) none of the above
35. Property of locality of reference may fail if a program has
(a) many conditional jumps (b) many unconditional jumps
(c) many operands (d) none of the above
36. Which of the following comments about half adder are true?
(a) It adds 2 bits.
(b) It is called so because a full adder involves two half-adders.
(c) It does half the work of a full adder.
(d) It needs two input and generates two output.
37. The binary equivalent of the decimal number 0.4375 is
(a) 0.0111 (b) 0.1011 (c) 0.1100 (d) 0.1010
- *38. The Boolean expression $(A + C)(AB' + AC)(A'C' + B')$ can be simplified to
(a) AB (b) $AB + A'C$ (c) $A'B + BC$ (d) $AB + BC$
- *39. A byte addressable computer has a memory capacity of 2^m kbytes and can perform 2^n operations. An instruction involving 3 operands and one operator needs a maximum of
(a) $3m$ bits (b) $3m + n$ bits (c) $m + n$ bits (d) none of the above
- *40. In the previous problem, if the computer is word addressable with the word size being 8 bytes then the answer will be
(a) $3m$ bits (b) $3m + n$ bits (c) $m + n$ bits (d) none of the above

- *41. The number of columns in a state table for a sequential circuit with ' m ' flip-flops and ' n ' input is
 (a) $m + n$ (b) $m + 2n$ (c) $2m + n$ (d) $2m + 2n$
42. A computer uses ternary system instead of the traditional binary system. An ' n ' bit string in the binary system will occupy
 (a) $3 + n$ ternary digits (b) $2n/3$ ternary digits
 (c) $n(\log_2 3)$ ternary digits (d) $n(\log_3 2)$ ternary digits
- *43. The Boolean expression $A'BE + BCDE + BC'D'E + A'B'DE' + B'C'DE'$ can be simplified to $BE + B'DE'$, if the don't care conditions are
 (a) $ABCDE + AB'CDE'$ (b) $ABCD + AB'CDE' + ABCD'E$
 (c) $ABC'DE + AB'CDE' + ABCD'E$ (d) none of the above
44. The decimal equivalent of the binary number 101.101 is
 (a) 5.6249 (b) 5.625 (c) 5.5 (d) 5.25
45. Which of the following does not have 8 data lines?
 (a) 8085 (b) 8086 (c) 8088 (d) Z-80
46. Which of the following logic families is well suited for high-speed operation?
 (a) TTL (b) ECL (c) MOS (d) CMOS
47. The following arrangement of JK flip-flops does the function of a

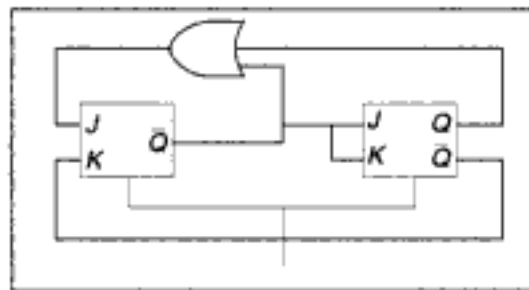


Fig. 8.1

- (a) Shift register (b) Mod-3 counter (c) Mod-2 counter (d) none of the above
48. Negative numbers cannot be represented in
 (a) signed magnitude form (b) 1's complement form
 (c) 2's complement form (d) none of the above
49. The addressing mode used in an instruction of the form $ADD\ X\ Y$, is
 (a) absolute (b) immediate (c) indirect (d) index
- *50. The combinational circuit in Fig. 8.2 can be replaced by a single
 (a) OR gate (b) XOR gate
 (c) NOR gate (d) AND gate
- *51. $(10110011100011110000)_2$ in base 32 is
 (a) 22 14 7 16 (b) 11 9 23 31 (c) 11 9 7 16 (d) 11 14 23 16

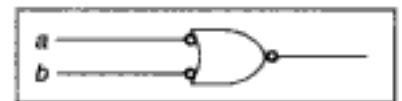


Fig. 8.2

- *52. The XOR operator \oplus is
 (a) commutative (b) associative
 (c) distributive over AND operator (d) none of the above
53. Bubble memories are preferable to floppy disks because
 (a) of their higher transfer rate (b) the cost needed to store a bit is less
 (c) they consume less power (d) of their reliability
54. Addressing capability of 8086/88 is
 (a) 64 K (b) 512 K (c) 2 MB (d) 1 MB
55. The following circuit produces the output sequence

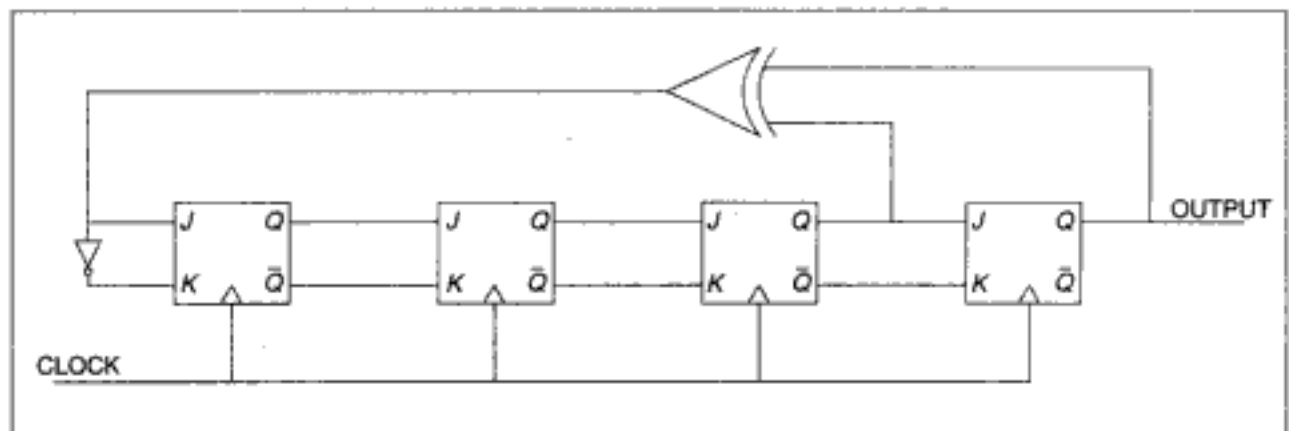


Fig. 8.3

- (a) 1111 1111 0000 0000 (b) 1111 0000 1111 000
 (c) 1111 0001 0011 010 (d) 1010 1010 1010 1010
56. Which of the following units can be used to measure the speed of a computer?
 (a) SYPS (b) MIPS (c) BAUD (d) FLOPS
- *57. if $A \oplus B = C$ (\oplus stands for the XOR operator), then
 (a) $A \oplus B = B$ (b) $B \oplus C = A$
 (c) $A \oplus B \oplus C = 0$ (d) none of the above
58. Which of the following operation(s) is/are not closed as regards to computers?
 (a) Addition (b) Subtraction (c) Multiplication (d) Division
- *59. If $(11A1B)_8 = (12C9)_{16}$ (C stands for decimal 12), then the values of A and B are
 (a) 5, 1 (b) 7, 5 (c) 5, 7 (d) none of the above
- *60. The total number of possible Boolean functions involving 'n' Boolean variables is
 (a) infinitely many (b) n^n (c) n^2 (d) none of the above
61. Which of the following architecture is/are not suitable for realizing SIMD?
 (a) Vector processor (b) Array processor
 (c) Von Neumann (d) All of the above

- *62. How many 2-input multiplexers are required to construct a 2^{10} -input multiplexer?
 (a) 1023 (b) 31 (c) 10 (d) 127
- *63. Let A be a set having 'n' elements. The number of binary operations that can be defined on A is
 (a) n^{n^2} (b) 2^{n^2} (c) n^{2^n} (d) 2^{2^n}
- *64. The values of x and y, if $(x567)_8 + (2yx5)_8 = (71yx)_8$ is
 (a) 4, 3 (b) 3, 3 (c) 4, 4 (d) 4, 5
- *65. A decimal number has 25 digits. The number of bits needed for its equivalent binary representation is, approximately,
 (a) 50 (b) 60 (c) 70 (d) 75
- *66. The number of instructions needed to add 'n' numbers and store the result in memory using only one address instructions is
 (a) n (b) n - 1 (c) n + 1 (d) independent of n
- *67. The Boolean expression corresponding to the circuit in Fig. 8.4 is

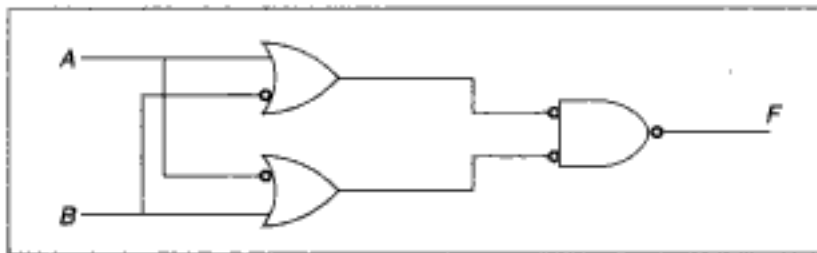


Fig. 8.4

- (a) a tautology (b) an inconsistency
 (c) independent of A (d) none of the above
68. The clock of a microprocessor can be divided by 5 using a
 (a) 3 bit counter (b) 5 bit counter (c) mod 5 counter (d) mod 3 counter
- *69. The minimal cover for the maximal compatibility classes {ae, acd, ad, bd} is
 (a) ae, acd, ad (b) acd, ad, bd
 (c) ae, acd, bd (d) ae, ad, bd
- *70. The values of a, x, y if $47x80$ is the 10's complement of $yaya0$ are
 (a) 4, 3, 2 (b) 5, 4, 4 (c) 3, 4, 5 (d) 2, 4, 5
71. The reasons for the presence of ALE pin in 8085, but not in 6800 is that
 (a) 8085 uses I/O mapped I/O, whereas 6800 uses memory mapped I/O
 (b) 8085 has 5 interrupt lines, whereas 6800 has only 2
 (c) 8085 has multiplexed bus, whereas 6800 doesn't have
 (d) none of the above
- *72. If memory access takes 20 ns with cache and 110 ns without it, then the hit-ratio, (cache uses a 10 ns memory) is,
 (a) 93% (b) 90% (c) 87% (d) 88%

73. In which of the following instructions bus idle situation occurs?
 (a) EI (b) DAD rp (c) INX H (d) DAA
- *74. Any instruction should have at least
 (a) 2 operands (b) 1 operand (c) 3 operands (d) none of the above
- *75. Consider the circuit in Fig. 8.5.

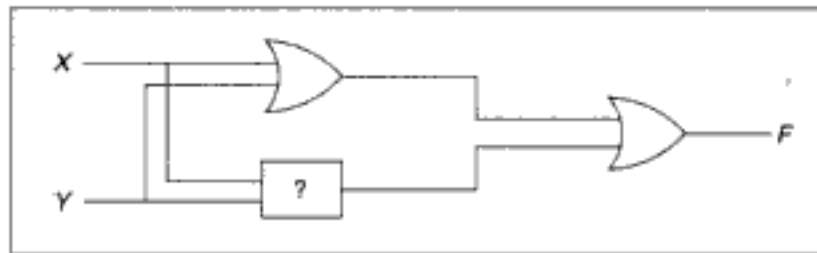


Fig. 8.5

- In order to make it a tautology the '?' marked box should be replaced by
 (a) an OR gate (b) an AND gate (c) a NAND gate (d) a NOR gate
- *76. If the cache needs an access time of 20 ns and the main memory 120 ns, then the average access time of a CPU is (assume hit-ratio is 80%)
 (a) 30 ns (b) 40 ns (c) 35 ns (d) 45 ns
77. The number of clock cycles necessary to complete 1 fetch cycle in 8085 (excluding wait state) is
 (a) 3 or 4 (b) 4 or 5 (c) 4 or 6 (d) 3 or 5
- *78. The seek time of a disk is 30 ms. It rotates at the rate of 30 rotations per second. Each track has a capacity of 300 words. The access time is approximately
 (a) 47 ms (b) 50 ms (c) 60 ms (d) 62 ms
79. Motorola's 68040 is comparable to
 (a) 8085 (b) 80286 (c) 80386 (d) 80486
- *80. The possible number of Boolean functions of 3 variables X, Y and Z such that $f(X, Y, Z) = f(X', Y', Z')$ is
 (a) 8 (b) 16 (c) 64 (d) 32
81. Which of the following interrupt is both level and edge sensitive?
 (a) RST 5.5 (b) INTR (c) RST 7.5 (d) TRAP
82. The difference between 80486 and 80386 is/are
 (a) presence of floating point co-processor
 (b) speed of operation
 (c) presence of 8 K cache on chip
 (d) presence of memory controller
83. The addressing mode used in the instruction `PUSH B` is
 (a) direct (b) register (c) register indirect (d) immediate

84. The most relevant addressing mode to write position independent code is
(a) direct mode (b) indirect mode (c) relative mode (d) indexed mode
85. Which of the following are CISC machines?
(a) IBM 360 (b) 80386 (c) 68030 (d) none of the above
86. Which of the following rules regarding the addition of 2 given numbers is correct, if negative numbers are represented in 2's complement form?
(a) Add sign bit and discard carry, if any.
(b) Add sign bit and add carry, if any.
(c) Don't add sign bit and discard carry, if any.
(d) Don't add sign bit and add carry, if any.
87. When INTR is encountered, the processor branches to the memory location, which is
(a) 0024H
(b) determined by the 'call address' instruction issued by the I/O device
(c) determined by the 'RST n' instruction issued by the I/O device
(d) all of the above
88. The advantage of a single bus over a multi-bus is the
(a) low cost (b) flexibility in attaching peripheral devices
(c) high operating speed (d) all of the above
- *89. The number of possible Boolean functions that can be defined for n Boolean variables over n -valued Boolean algebra is
(a) 2^{2^n} (b) 2^{n^2} (c) n^{2^n} (d) n^{n^n}
90. The ASCII code 56, represents the character
(a) V (b) 8 (c) a (d) carriage return
91. Parallel printer uses
(a) RS-232C interface (b) centronics interface
(c) hand-shake mode (d) synchronous data transfer mode
92. A microprogrammed control unit
(a) is faster than a hard-wired control unit
(b) facilitates easy implementation of new instructions
(c) is useful when very small programs are to be run
(d) usually refers to the control unit of a microprocessor
93. Which of the following are typical characteristics of a RISC machine?
(a) Instruction taking multiple cycles
(b) Highly pipelined
(c) Instructions interpreted by microprograms
(d) Multiple register sets
- *94. The working of a staircase switch is a typical example of the logical operation
(a) OR (b) NOR (c) Exclusive-OR (d) Exclusive-NOR

95. The exponent of a floating-point number is represented in excess-N code so that
- the dynamic range is large
 - the precision is high
 - the smallest number is represented by all zeroes
 - overflow is avoided
96. On receiving an interrupt from an I/O device, the CPU
- halts for a predetermined time
 - hands over control of address bus and data bus to the interrupting device
 - branches off to the interrupt service routine immediately
 - branches off to the interrupt service routine after completion of the current instruction.

- *97. The Karnaugh map for the Boolean function F of 4 Boolean variables is given in Fig. 8.6. A, B, C are don't care conditions. What values of A, B, C , will result in the minimal expression?

- $A = B = C = 1$
- $B = C = 1; A = 0$
- $A = C = 1; B = 0$
- $A = B = 1; C = 0$

		A	
	1	1	
1	B	C	
		1	

Fig. 8.6

98. In serial communication, an extra clock is needed
- to synchronize the devices
 - for programmed baud rate control
 - to make efficient use of RS-232
 - none of the above
99. If negative numbers are stored in 2's complement form, the range of numbers that can be stored in 8 bits is
- 128 to +128
 - 128 to +127
 - 127 to +128
 - 127 to +127
100. If SUB A, B means $B - A$, then SUB 4(R0), *5(R1) means (X) means content of register or memory location X)
- $((R1) + 5) - (4 * (R0))$
 - $((R1) + 5) - ((R0) + 4)$
 - $((R1) + 5) - (4 * (R0))$
 - $((R1) + 4) - (R0 + 4)$
- *101. A computer uses a floating-point representation comprising a signed magnitude fractional mantissa and an excess-16 base-8 exponent. What decimal number is represented by a floating-point number whose exponent is 10011, mantissa 101000, and the sign bit set?
- 6250
 - 20480
 - 320
 - 0.00122
102. The binary equivalent of the Gray code 11100 is
- 10111
 - 00111
 - 01011
 - 10101
- *103. The minimum number of 2-input NAND gates required to implement the function $F = (x' + y')(z + w)$ is
- 3
 - 4
 - 5
 - 6

113. An assembler that runs on one machine but produces machine code for another machine is called
 (a) simulator (b) emulator (c) cross-assembler (d) boot-strap loader
114. When even-parity ASCII text is transmitted asynchronously at a rate of 10 characters per sec over a 110-bps line, what percentage of the received bits actually contain data (as opposed to overhead)?
 (a) 7/11 (b) 8/11 (c) 700/11 (d) 80/11
115. Which of the following is not typically found in the status register of a microprocessor?
 (a) Overflow (b) Zero result (c) Negative result (d) None of the above
116. The output F , of the circuit given in Fig. 8.8 is given by

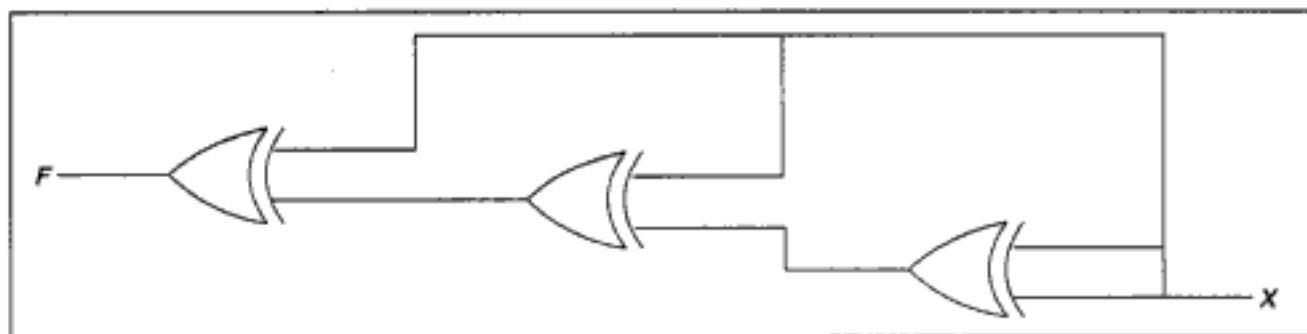


Fig. 8.8

- (a) 1 (b) 0 (c) X (d) X'
117. Most of the digital computers do not have floating-point hardware because
 (a) it is costly
 (b) it is slower than software
 (c) floating-point addition cannot be performed by hardware.
 (d) none of the above
118. ' n ' flip-flops will divide the clock frequency by a factor of
 (a) n^2 (b) n (c) 2^n (d) $\log(n)$
119. A toggle operation cannot be performed using a single
 (a) NOR gate (b) AND gate (c) NAND gate (d) XOR gate
120. Micro program is
 (a) the name of a source program in micro computers
 (b) the set of instructions indicating the primitive operations in a system
 (c) a primitive form of macros used in assembly language programming
 (d) a program of very small size
121. The three main components of a digital computer system are
 (a) memory, I/O, DMA (b) ALU, CPU, memory
 (c) memory, CPU, I/O (d) control circuits, ALU, registers

- *122. A subtractor is not usually present in a computer because
- it is expensive
 - it is not possible to design it
 - the adder will take care of subtraction
 - none of the above
- *123. Let $a_n a_{n-1} \dots a_1 a_0$ be the binary representation of an integer b . The integer b is divisible by 3 if
- the number of one's is divisible by 3
 - the number of one's is divisible by 3, but not by 9
 - the number of zeroes is divisible by 3
 - the difference of alternate sum, i.e., $(a_0 + a_2 + \dots) - (a_1 + a_3 + \dots)$ is divisible by 3
124. Which of the following 4-bit numbers equals its 2's complement?
- 1010
 - 0101
 - 1000
 - No such number exists
- *125. Which of the following 4-bit numbers equals its 1's complement?
- 1010
 - 1000
 - No such number exists
 - None of the above
- *126. FFFF will be the last memory location in a memory of size
- 1 k
 - 16 k
 - 32 k
 - 64 k
127. If you want to design a boundary counter, you should prefer a flip-flop of
- D-type
 - SR-type
 - latch
 - JK type
- *128. Suppose the largest n -bit binary number requires ' d ' digits in decimal representation. Which of the following relations between ' n ' and ' d ' is approximately correct?
- $d = 2^n$
 - $n = 2^d$
 - $d < n \log_{10} 2$
 - $d > n \log_{10} 2$
- *129. A computer uses 8-digit mantissa and 2-digit exponent. If $a = 0.052$ and $b = 28E + 11$, then $b+a-b$ will
- result in an overflow error
 - result in an underflow error
 - be 0
 - be $5.28E+11$
130. In Question 129, ' a ' will actually be stored as (the '/' is separating the mantissa and the exponent)
- 00000000/00
 - 05200000/00
 - 52000000/-09
 - 52000000/-01
131. Which of the following binary numbers are not divisible by 4?
- 10101010101010
 - 100101100
 - 1110001110001
 - 1111000011
132. A computer with a 32-bit wide data bus uses $4 K \times 8$ static RAM memory chips. The smallest memory this computer can have is
- 32 Kb
 - 16 Kb
 - 8 Kb
 - 24 Kb

161. MVI B, 00
 MVI A, 1cH
 DCR B
 DAA
 STA TEMP
 HLT

The content of the TEMP location after the execution of the above program is

- (a) 1Ch (b) 22h (c) 82h (d) 12h

162. Which of the following instructions requires the most number of T-states?

- (a) MOV A, B (b) MOV A, M (c) LDAX B (d) DAD D

163. Consider the following program. Assume that the program is stored in R/W memory.

```
Initial condition: (A000H) = 00H
8000: 31 07 80 LXI SP, 8007H
8003: 3E 76 MVI A, 76H
8005: F5 PUSH PSW
8006: 3A 00 A0 LDA A000H
8009: F1 POP PSW
800A: 3A 00 A0 STA A000H
800D 76 HLT
```

The content of the location A000H after the execution of the above program is

- (a) 76h (b) 00h (c) FFh (d) 55h

164. The 8085 μP enters into wait state after the recognition of

- (a) HOLD (b) *READY (c) *RESET-IN (d) INTR

165. Maximum number of I/O devices that can be addressed by Intel 8085 is

- (a) 65,536 (b) 255 (c) 512 (d) 256

166. The μP may be made to exit from HALT state by asserting

- (a) RESET (b) any of the five interrupt lines
 (c) READY line (d) option (a) or option (b) or HOLD line

167. The number of RAM chips of size (256 K \times 1) required to build a 1 Mbyte memory is

- (a) 8 (b) 32 (c) 10 (d) 24

168. 8000: 31 07 80 LXI SP, 8007H
 8003: AF XRA A
 8004: FE 0A CPI 0AH
 8006: D8 RC
 8007: 0C INR C
 8008: 80 ADD B
 8009: 02 STAX B

```

block
      MVI C, 05H ; count = 5
LOOP : MOV A, M
      STAX B ; block copy
      INX X
      INX H
      DCR C
      JNZ LOOP
      HLT

```

- (a) JNZ instruction is used instead of JZ
 (b) C register is used as counter
 (c) the starting address of the destination block is altered as 9005H
 (d) DCR C instruction will not affect zero flag
- 181.** RST 3 instruction will cause the processor to branch to the location
 (a) 0000h (b) 0018h (c) 0024h (d) 8018h
- 182.** Which one of the following interrupts is non-maskable?
 (a) TRAP (b) RST 7.5 (c) INTR (d) RST 6.5
- 183.** Which one of the following instructions will never affect the zero flag?
 (a) DCR reg (b) ORA reg (c) DCX rp (d) XRA reg
- 184.** The contents of the A15-A8 (higher order address lines) while executing *IN addr* instruction are
 (a) same as the contents of A7-A0 (b) irrelevant
 (c) all bits reset (i.e. 00h) (d) all bits set (i.e. FFh)
- 185.** Which of the following peripheral ICs is used to interface keyboard and display?
 (a) 8251 (b) 8279 (c) 8259 (d) 8253
- 186.** The only interrupt that is edge-triggered is
 (a) INTR (b) TRAP (c) RST 7.5 (d) RST 5.5
- 187.** Which one of the following instructions may be used to clear the accumulator content (i.e. A = 00h) irrespective of its initial value?
 (a) CLR A (b) ORA A (c) SUB A (d) MOV A, 00h
- 188.** The execution of RST n instruction causes the stack pointer to
 (a) increment by two (b) decrement by two
 (c) remain unaffected (d) none of the above
- 189.** The stack is nothing but a set of
 (a) reserved ROM address space (b) reserved RAM address space
 (c) reserved I/O address space (d) none of the above
- 190.** The instruction used to shift right the accumulator contents by one bit through the carry flag bit is
 (a) RLC (b) RAL (c) RRC (d) RAR

191. The minimum number of bits required to represent a character from ASCII code set is
 (a) 2 (b) 5 (c) 7 (d) 8

192. Consider the following program fragment

```

DELAY:   LXI H, 0010H
LOOP:   DCX H
        MOV A, L
        ORA H
        XRA A
        JNZ LOOP
        RET
  
```

The number of times LOOP will be executed is

- (a) 16 (b) 10 (c) 1 (d) infinite

193. 8000: START: LXI H, 0001H
 LXI D, 8010H
 XCHG
 DCX D
 JZ 800C
 PCHL
 800 C: JMP 8000
 NOP
 HLT

Referring to the above program, which of the following statements is true?

- (a) The program will loop infinitely
 (b) The program will reach halt state after the first pass
 (c) The program will reach halt state after 8010h times
 (d) None of the above
194. S0 and S1 pins are used for
 (a) serial communication (b) indicating the processor's status
 (c) acknowledging the interrupt (d) none of the above
195. Pick out the matching pair.
 (a) READY; RIM (b) HOLD; DMA
 (c) SID; SIM (d) S0, S1; Wait states
197. Consider the following program:

```

          ORG 8000H
START:   LXI H, 8000H
          MOVE A, L
          ADD H
          JM XYZ
          RST 0
  
```

```

XYZ:   PCHL
       HLT

```

Pick out the correct statement from the following:

- (a) the program will branch to 0000H after JM XYZ
 - (b) the program will branch to 0008H after JM XYZ
 - (c) the program will halt the processor
 - (d) the program will be repeated infinitely
- 198.** Assume that the 8255 gets selected whenever A15-A11 are high during I/O read or write cycles. The A2 and A1 are connected to A1 and A0 of 8255 chip. Then, the address for port C of 8255 is
- (a) 03h
 - (b) FEh
 - (c) FFh
 - (d) FF03h
- 199.** Assume that a slow memory device is interfaced with an 8085 microprocessor and an 1-wait state generating circuit is connected to READY input. Then, the execution time needed for the following program would be,
- ```

LDA TEMP
ADD B
LHLD TEMP

```
- (a) 43 T-states
  - (b) 30 T-states
  - (c) 40 T-states
  - (d) 33 T-states
- 200.** Which of the following instructions may be used to save the accumulator value onto the stack?
- (a) PUSH PSW
  - (b) PUSH A
  - (c) PUSH SP
  - (d) POP PSW
- 201.** A single instruction to clear the lower four bits of the accumulator in 8085 assembly language is
- (a) XRI 0FH
  - (b) ANI 0FH
  - (c) XRI F0H
  - (d) ANI 0FH
- 202.** Which of the following statements is true?
- (a) ROM is a read/write memory.
  - (b) PC points to the last instruction that was executed.
  - (c) Stack works on the principle of LIFO.
  - (d) All instructions affect the flag.
- 203.** In a vectored interrupt the
- (a) branch address is assigned to a fixed location in memory.
  - (b) interrupting source supplies the branch information to the processor through an interrupt vector
  - (c) branch address is obtained from a register in the processor
  - (d) none of the above
- 204.** A sequence of two instructions that multiplies the contents of the DE register pair by 2 and stores the result in the HL register pair (in 8085 assembly language) is
- (a) XCHG and DAD B
  - (b) XTHL and DAD H
  - (c) PCHL and DAD D
  - (d) XCHG and DAD H

- (c) is useful when small programs are to be run  
 (d) all of the above

215. The output of the multiplexer circuit in Fig. 8.9 can be represented by  
 (a)  $AB + BC' + C'A + BC$   
 (b)  $A + B + C$   
 (c)  $A + B$   
 (d)  $A'B'C + A'BC' + ABC$

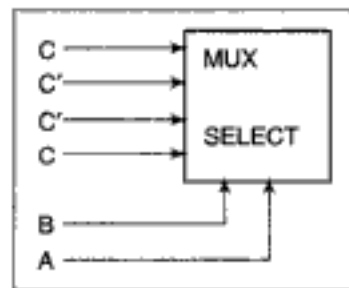


Fig. 8.9

216. In a 11 bit computer instruction format, the size of address field is 4 bits. The computer uses expanding OP code technique and has 5 two-address instructions and 32 one-address instructions. The number of zero address instructions it can support is  
 (a) 256 (b) 2048 (c) 16 (d) 272
217. PCHL is an instruction in 8085 which transfers the contents of the register pair HL to PC. This is not a commonly used instruction as it changes the flow of control in a rather unstructured fashion. This instruction cannot be used in implementing.  
 (a) if... then ... else construct  
 (b) while ... do construct  
 (c) case ... structure  
 (d) call ... statement
218. To change an upper case character to a lower case character in ASCII, the correct mask and operation should be  
 (a) 0100000 and NOR (b) 0100000 and OR  
 (c) 0100000 and NAND (d) 1011111 and AND
219. The number of flip-flops needed to construct a binary modulo N counter is  
 (a) N (b)  $2^N$  (c)  $N^2$  (d)  $\log_2 N$
220. Multiplexing of data/address lines in an 8085 microprocessor reduces the instruction execution time. This statement is  
 (a) true (b) false  
 (c) most likely to be true (d) none of the above
221. Which of the following is unipolar, difficult to fabricate, has very high speed and offers good resistance to radiation?  
 (a) ECL (b) GaAs (c) TTL (d) CMOS
222. What is  $A*A$ , if \* is a Boolean operation defined by  $A*B = AB + A'B'$ ?  
 (a) A (b) B (c) 0 (d) 1
223. If  $C = A*B$ , then  $C*A$  is  
 (a) A (b) B (c) 0 (d) 1
224. The Boolean variables A, B and C, that solve the Boolean equations  $AB + A'C = 1$  and  $AC + B = 0$  simultaneously is  
 (a) 1, 0, 0 (b) 0, 1, 1 (c) 1, 0, 1 (d) 0, 0, 1

225. If a particular idea can be implemented in hardware or software, the factor(s) that favour hardware implementation is/are
- (a) cost-effectiveness (b) speed of operation  
(c) reliability (d) frequent changes expected
226. Tera is 2 to the power of
- (a) 32 (b) 30 (c) 40 (d) 25
227. Von Neumann architecture is
- (a) SISD (b) SIMD (c) MIMD (d) MISD
- \*228. To achieve parallelism, one needs a minimum of
- (a) 2 processors (b) 3 processors  
(c) 4 processors (d) none of the above
229. SIMD can be used for
- (a) railway reservation (b) weather forecasting  
(c) matrix multiplication (d) all of the above
230. A typical application of MIMD is
- (a) railway reservation (b) weather forecasting  
(c) matrix multiplication (d) all of the above
- \*231. Let \* be a defined as  $a*b = a' + b$ . Let  $m = a*b$ . The value of  $m*a$  is
- (a)  $a' + b$  (b)  $a$  (c) 0 (d) 1
232. The correct matching for the following pairs is
- (A) DMA I/O (1) High speed RAM  
(B) Cache (2) Disk  
(C) Interrupt I/O (3) Printer  
(D) Condition Code Register (4) ALU
- (a) A-4, B-3, C-1, D-2 (b) A-2, B-1, C-3, D-4  
(c) A-4, B-3, C-2, D-1 (d) A-2, B-3, C-4; D-1
233. Contents of A register after the execution of the following 8085 microprocessor program is
- MVI A, 55h  
MVI C, 25h  
ADD C  
DAA
- (a) 7Ah (b) 80h (c) 50h (d) 22h
234. RST 7.5 interrupt in 8085 microprocessor executes service routine from interrupt vector location
- (a) 0000h (b) 0075h (c) 003Ch (d) 0034h

**Answers**

- |              |                |                |                |                |
|--------------|----------------|----------------|----------------|----------------|
| 1. c         | 2. b, c, d     | 3. a, c        | 4. c, d        | 5. a           |
| 6. a, c      | 7. b           | 8. b, c        | 9. a, c        | 10. d          |
| 11. a, b     | 12. d          | 13. b, c, d    | 14. c          | 15. a, b, c    |
| 16. a        | 17. b, c       | 18. a, b, c    | 19. a, c, d    | 20. c          |
| 21. b, d     | 22. a, b, c    | 23. c          | 24. a, b, c, d | 25. a, b       |
| 26. b, c     | 27. c          | 28. a, b, c, d | 29. c          | 30. a          |
| 31. a, b     | 32. c          | 33. b          | 34. d          | 35. a, b, c    |
| 36. a, b, d  | 37. a          | 38. a          | 39. d          | 40. d          |
| 41. c        | 42. d          | 43. c          | 44. b          | 45. b          |
| 46. b        | 47. b          | 48. d          | 49. a          | 50. a          |
| 51. a        | 52. a, b       | 53. c, d       | 54. d          | 55. c          |
| 56. b, d     | 57. a, b, c    | 58. a, b, c, d | 59. d          | 60. d          |
| 61. c        | 62. a          | 63. a          | 64. a          | 65. d          |
| 66. c        | 67. a          | 68. c          | 69. c          | 70. d          |
| 71. c        | 72. b          | 73. b          | 74. d          | 75. c, d       |
| 76. b        | 77. c          | 78. a          | 79. d          | 80. b          |
| 81. d        | 82. a, b, c, d | 83. c          | 84. c          | 85. a, b, c, d |
| 86. a        | 87. b, c       | 88. a, b       | 89. d          | 90. b          |
| 91. b, c     | 92. b          | 93. b, d       | 94. c          | 95. c          |
| 96. d        | 97. d          | 98. b          | 99. b          | 100. b         |
| 101. c       | 102. a         | 103. b         | 104. b         | 105. c         |
| 106. c       | 107. b         | 108. b         | 109. b         | 110. a         |
| 111. d       | 112. a         | 113. c         | 114. c         | 115. d         |
| 116. b       | 117. a         | 118. c         | 119. b         | 120. b         |
| 121. c       | 122. c         | 123. d         | 124. c         | 125. c         |
| 126. d       | 127. a         | 128. d         | 129. c         | 130. d         |
| 131. a, c, d | 132. b         | 133. a, c      | 134. d         | 135. c         |
| 136. b       | 137. b         | 138. a         | 139. d         | 140. c         |
| 141. b       | 142. a, b      | 143. c         | 144. b, d      | 145. a         |
| 146. c       | 147. b         | 148. a         | 149. a         | 150. d         |
| 151. a       | 152. b         | 153. a         | 154. c         | 155. c         |
| 156. b       | 157. c         | 158. d         | 159. c         | 160. c         |
| 161. b       | 162. d         | 163. b         | 164. b         | 165. d         |
| 166. d       | 167. b         | 168. c         | 169. b, c      | 170. b         |
| 171. b       | 172. d         | 173. c         | 174. a         | 175. d         |
| 176. a       | 177. b         | 178. b         | 179. a         | 180. b, c      |

|        |        |           |           |           |
|--------|--------|-----------|-----------|-----------|
| 181. b | 182. a | 183. c    | 184. a    | 185. b    |
| 186. c | 187. c | 188. b    | 189. b    | 190. d    |
| 191. c | 192. c | 193. b    | 194. b    | 195. b    |
| 196. b | 197. d | 198. b, c | 199. a    | 200. a    |
| 201. b | 202. c | 203. a    | 204. d    | 205. c    |
| 206. a | 207. c | 208. d    | 209. d    | 210. d    |
| 211. a | 212. c | 213. c    | 214. b    | 215. b    |
| 216. a | 217. d | 218. b    | 219. d    | 220. b    |
| 221. b | 222. d | 223. b    | 224. d    | 225. b, c |
| 226. c | 227. a | 228. d    | 229. b, c | 230. a    |
| 231. b | 232. b | 233. b    | 234. c    |           |

## Explanations

- Exclusive OR takes the value 0 if there are even number of 1's.
- X can take the value of either 1 or 0. Substitute and verify the identities.
- Form truth table and check the correctness of the options (c) and (d).
- Substitute and verify each of the possibilities.
- During execution of the current instruction the content is incremented so that it points to the next instruction.
- Converting to decimal form, the given equation is  
 $3 + (2 \times 5) + (1 \times 5 \times 5) = 3 + A \times B$  i.e.,  $38 = A \times B + 3$ . So,  $A \times B = 35$ . Possible values for A, B are 1, 35; 5, 7; 7, 5; 35, 1.  
 7, 5 and 35, are infeasible, as permissible digits for a number in base 'r' are 0, 1, 2, ... (r-1). Hence 1 and 5 are the possible values of A.
- Refer Qn. 10. Converting to decimal form,  $A + 2 \times 3 + 1 \times 3 \times 3 = 3 + 2 \times A + 1 \times A \times A$ . Solving for A, we get  $A = -4$  or 3. Both are infeasible.
- The contents of a word may represent an instruction or data. Just by looking at the contents, it is not possible to attach any meaning to it. A word pointed to by the program counter, is an instruction. Otherwise it need not be. Also, the word data has context sensitive meaning. One can write a program in Pascal that needs radius as the input data. The program, as a whole, is input data for the compiler during the compilation process.
- $$X + X'Y = X \cdot 1 + X'Y = X(1 + Y) + X'Y = X \cdot 1 + XY + X'Y$$

$$= X + (X + X')Y = X + 1 \cdot Y = X + Y$$
 If that sounds quite unnatural, here is another way. Let  $K = X + X'Y$  (we have to find K)  
 Complementing both sides  $K' = (X + X'Y)' = X' \cdot (X + Y')$   

$$= X'X + X'Y' = 1 + X'Y'$$

$$= X'Y'$$
 Again complementing both sides  $K = (X'Y')' = X + Y$   
 Hence the answer is (a).

17. Obviously it shows it is associative. It implies (by the law of duality), the associativity of AND also. Complementing both sides,

$$\begin{aligned}(X + (Y + Z))' &= ((X + Y) + Z)' \\ X'(Y'Z') &= (X'Y')Z'\end{aligned}$$

(By De Morgan's law)

22. Karnaugh map is just pictorial representation of a truth table. By covering the 1's, we get the sum of product form. By covering the 0's and then complementing, we get the product of sum form.
23. Consider the decimal digit 5. Its BCD representation is 0101. If complemented, we get 1010, i.e., 15 - 5. In general, complementing  $x$  gives  $15 - x$ . But correct complemented value should be  $9 - x$ . The difference of 6 can be nullified by going for excess-3 code. (3 because using it twice, i.e., during the conversion and reversion process one can account for the excess 6.) If a number system uses 20 as the radix, each digit needs 5 bits in the equivalent BCD form. So, complement of  $x$ , gives  $31 - x$ . But the correct value is  $19 - x$ . To account for the excess  $31 - 19$ , i.e., 12, we have to use excess-6 code. e.g., take 11. Its complement should be  $19 - 11 = 8$ . In excess-6 code, we add 6 to 11, to get 17. Complementing, we get  $31 - 17 = 14$ . If we subtract the excess 6, we get  $14 - 6 = 8$ , which is the required answer.
25. By NAND gate as follows.

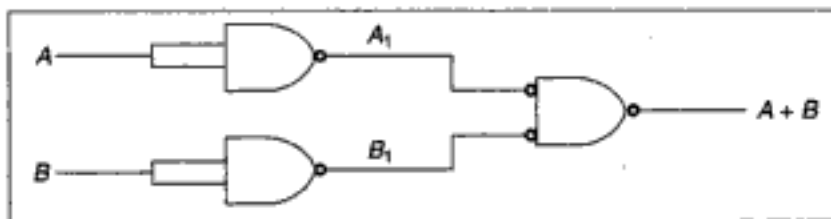


Fig. 8.10(a)

By NOR gate as follows.



Fig. 8.10(b)

28. 90 - 10 is a heuristic rule that says 90% of the execution time is spent on 10% of the code.
29. Consider the decimal digit 5. Its BCD form is 0101. Complementing, we get 1010, which is decimal 10. To make 1010 correspond to decimal 4 (which is the correct complement of 5), we can assign the weights 2-4-2-1. This way 1010, will be decimal 4.
31. NOR and NAND are universal gates.

NAND can be simulated by NOR as follows.

$$\text{NAND}(A, B) = A' + B'$$

$$\text{NOR}(A, A) = A'$$

$$\text{NOR}(B, B) = B'$$

$$\text{NOR}(A', B') = (A' + B')' = AB$$

$$\text{NOR}(AB, AB) = (AB)' = A' + B' = \text{NAND}(A, B)$$

So, it suffices to prove NAND is a universal gate.

If that is true, it should simulate any Boolean operator. Since the basic operations are OR, AND, and complementation, it is enough to prove NAND can simulate these.

Refer Qn. 25 to see how OR can be simulated.

It is simple to simulate complementation.

$$\text{NAND}(A, A) = A'$$

AND can be simulated as follows.

$$\text{NAND}(A, B) = (AB)'$$

$$\text{NAND}((AB)', (AB)') = AB$$

Hence the correct answers are (a) and (b).

32. Don't care conditions need or need not be present. If present, they need or need not be used. If they aid in the simplification process, we use them to our advantage. Otherwise they are literally don't care.
33.  $AB + AB' + A'C + AC = A(B + B') + (A' + A)C$   
 $= A(1) + (1)C = A + C$ , which is independent of B.
34. The given expression is  $AB + AB' + A'C = A(B + B') + A'C = A(1) + A'C$   
 $= A + A'C = A + C$  (Refer Qn. 16)

So, one needs just a single OR gate to implement the given Boolean expression.

38.  $(A + C)(AB' + AC) = AAB' + AAC + ACB' + CAC$   
 $= AB' + AC + CAB' + AC$  (Since  $X \cdot X = X$ )  
 $= AB' + CAB' + AC$  (Since  $X + X = X$ )

So the given Boolean expression is

$$\begin{aligned} (AB' + CAB' + AC)(A'C' + B') &= AB'A'C' + AB'B' + CAB'A'C' + CAB'B' \\ &\quad + ACA'C' + ACB' \\ &= 0 + AE' + 0 + CAB' + 0 + ACB' \\ &= AB' + ACB' = AB'(1 + C) = AB' \end{aligned}$$

39. To specify a particular operation, out of the  $2^n$  possible operations, one needs  $n$  bits. As the machine is byte addressable, to specify a particular byte we need  $(m + 10)$  bits (since  $2^{(m+10)}$  bytes are there). So 3 addresses and 1 operation needs  $3(m + 10) + n = 3m + n + 30$  bits.
40. Refer Qn. 39.  
 If it is word addressable, then the number of words is  $2^{(m+10)}$  divided by  $2^3$ , i.e.,  $2^{m+7}$  words. So, one needs  $3(m + 7) + n = 3m + n + 21$  bits.
41. It is  $2m + n$ . ' $n$ ' columns for the ' $n$ ' inputs;  $2m$  columns for storing the ' $m$ ' present states and ' $m$ ' next states.



43.

| DE | ABC |     |     |     |     |     |     |     |
|----|-----|-----|-----|-----|-----|-----|-----|-----|
|    | 000 | 001 | 011 | 010 | 110 | 111 | 101 | 100 |
| 00 |     |     |     |     |     |     |     |     |
| 01 |     |     | 1   | 1   | 1   | X   |     |     |
| 11 |     |     | 1   | 1   | X   | 1   |     |     |
| 10 | 1   | 1   |     |     |     |     | X   | 1   |

Fig. 8.11

The terms  $A'BE$  corresponds to  $A' = 0$ ;  $B = 1$ ;  $E = 1$ ;  $C = 0$  or  $1$ ;  $D = 0$  or  $1$ . Similarly mark all 1's and get the Karnaugh map as above. The 1's can be covered in the optimal way, if the slots marked X are set to 1's. So the three X's in the positions  $ABCD'E$ ,  $ABC'DE$ ,  $AB'CDE'$  are the don't care conditions to be set to 1 and used. Hence the answer is (c).

50. The circuit is  $(A'B')' = A + B$ . Hence the answer.

51. To convert to base 8, we group in 3's, because  $2^3 = 8$ .

To convert to base 16, we group in 4's, because  $2^4 = 16$ .

To convert to base 32, we group in 5's because  $2^5 = 32$ .

Grouping in 5's, from the right, we can get the answer.

52. It is commutative because  $A \oplus B = B \oplus A$

It is associative because  $(A \oplus B) \oplus C = A \oplus (B \oplus C)$

It is not distributive over AND because

$$A \oplus (B \text{ AND } C) = (A \oplus B) \text{ AND } (A \oplus C)$$

is not true. For e.g.,  $1 \oplus (0 \text{ AND } 1) = 1$

$$\text{But } (1 \oplus 0) \text{ AND } (1 \oplus 1) = 1 \text{ AND } 0 = 0$$

57.  $X + Y = 0$  (Construct the truth table and verify)

$$\text{So, } A \oplus B = C \quad \Rightarrow \quad A \oplus (A + B) = A \oplus C$$

$$\Rightarrow (A \oplus A) \oplus B = A \oplus C$$

$$0 \oplus B = A \oplus C$$

$$B = A \oplus C$$

Similarly, (b) and (c) can be proved.

59. Converting to base 2, the equation reads

$$001 \ 001 \ A \ 001 \ B = 0001 \ 0010 \ 1100 \ 1001$$

Here A, B stand for a group of binary digits. So, grouping the right hand side in 3's, from the right and matching corresponding groups in both the sides, we get  $B = 001$  and  $A = 011$ .

So,  $A=3$  and  $B=1$ .

60. A single Boolean variable can take the values either 0 or 1, i.e., 2 possible ways. So, 'n' Boolean variables can take  $2 \times 2 \times 2 \dots$  (n times) values, i.e.,  $2^n$  times. So, the truth table will have  $2^n$  rows. Each row can be assigned one of the 2 values 0 or 1. So, totally  $2^{2^n}$  functions are possible. So, none of the given choices is true.

Taking  $a=b=c=-1$  and  $d = -5/2$ ,  $ax+by+cz < d$  becomes  
 $-x-y-z < 5/2$ .

This is true if  $x=y=z=1$ . For all other Boolean combinations of  $x, y, z$ , this is false. Hence the correct option is (b).

105. Another name for Gray code is unit-distance code.

108. Option (b) is  $(A+B)(A+C) = AA + AC + BA + BC$   
 $= A + AC + BA + BC$   
 $= A(1 + C + B) + BC$   
 $= A + BC$

110. P is the carry and Q is the sum. Check it yourself.

122. Shift and add are the primitive operations.

123. For example consider 10101011. Number of 1's in even places is 1. Number of 1's in odd places is 4. The difference  $4 - 1$ , is divisible by 3. So, the binary number 10101011 (i.e. decimal 171) is divisible by 3, which is true.

125. There can't be any such number. Because, if such a number say  $x$ , exists then  $x+x' = 2^4 - 1$ , i.e.,  $x+x' = 15$ , (since  $x' = x$ ), which is not true for any integer  $x$ .

126. 64 K is  $2^{16}$  bytes. i.e.  $16^4$  bytes i.e., 10000 bytes in hex code.  
 So last accessible address is  $10000-1 = \text{FFFF}$ .

128. The largest ' $n$ ' bit binary number is  $2^n - 1$ . If its equivalent decimal number has ' $d$ ' digits then it has to be less than  $10^d$ . So,  $2^n - 1 < 10^d$ , i.e.  $2^n < 10^d$  (approximately), so  $d > n \log_{10} 2$ .

129. Addition will be performed first.  $a + b$  will evaluate to ' $b$ ' as the significant digits of ' $a$ ' will be lost when it is converted to exponent 11. So,  $a + b - b$  is  $b - b$ , which is 0.

131. If it is to be divisible by 4, then both the two least significant bits has to be 0. So, only option (b) is divisible by 4.

149. Frequency = 3 MHz. So, time per T-state =  $1/3 \text{ MHz} = 3.33 \times 10^{-7}$  sec. Number of T-states = 13.

Total time =  $13 \times 3.33 \times 10^{-7} = 4333 \text{ ns}$ .

208. If one CPU completes its operation before the other, the result will be its original value. If one CPU has already fetched the value of  $x$ , and is in the process of updating it and at this point of time the other CPU fetches the value of  $x$  (which will be same as the value fetched by the first CPU), the first CPU after manipulating it will store back the result in  $x$ . After this the second CPU will store its manipulated value, over-writing what is stored by the first CPU. So, the final value may be its original value +1 if the first CPU decremented  $x$ , its original value - 1, otherwise.

228. Even with a single processor, parallelism can be achieved by overlapping instruction fetch, decode, address calculation, operand fetch and execution of different instructions simultaneously.

231.  $m*a = (a*b)*a = (a'+b)*a = (a'+b)'*a = ab'+a = a(b'+1) = a$